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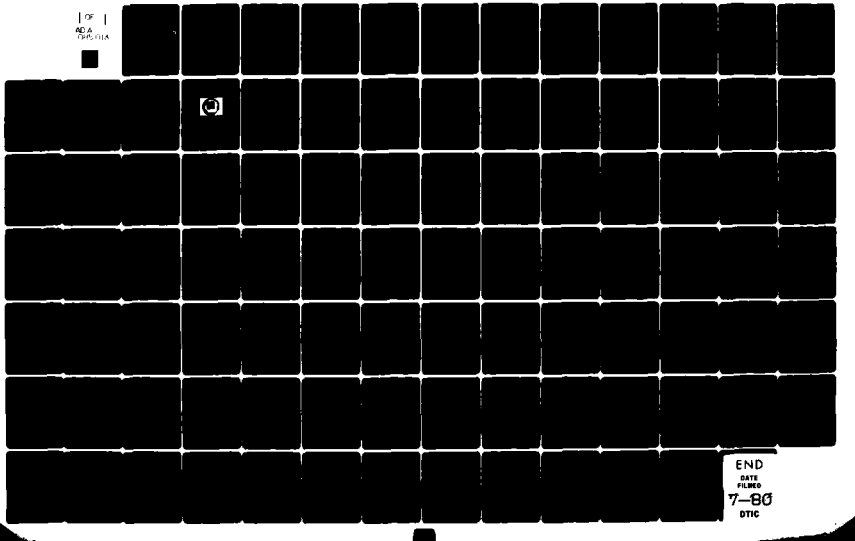

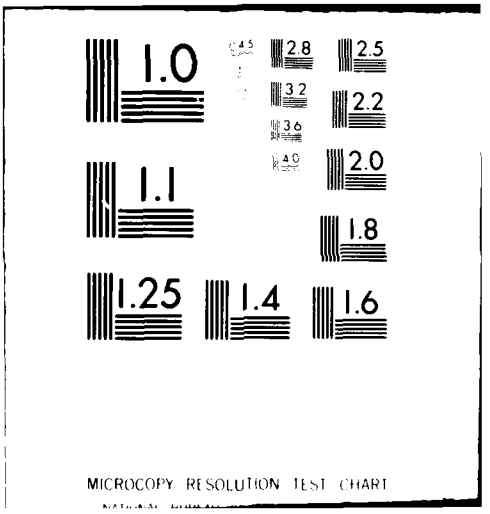
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PHASE I COMPLETION REPORT TOTAL DOSE HARDNESS ASSURANCE

Volume II: Verification Test Results

BDM Corporation
Albuquerque, NM 87106

February 1980

Final Report

This research was sponsored by the Defense Nuclear Agency under Subtask Z99QAXTD072, Work Unit 14, Hardness Assurance Techniques for LSI Devices.

Prepared for

Director
DEFENSE NUCLEAR AGENCY
Washington, DC 20305

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AFWL-TR-79-53, Vol. II

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report covers the first phase of a three phase program to develop hardness assurance techniques for the total ionizing radiation dose environment for bipolar and MOS semiconductor devices. Phase I consists of identifying and verifying potentially useful techniques. The report is presented in two volumes. Volume one discusses all of the potential hardness assurance techniques that were identified and whether or not they are sufficiently verified in previous studies. In addition, new techniques are proposed based on models of radiation-induced hole trapping and interface state generation. (over)

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Each technique identified or proposed is discussed in terms of its implementation, cost effectiveness, and acceptability. Recommendations are made for each technique to: a. reject for this program, b. verify its usefulness with further testing or, c. accept as useful and include in the evaluation phase. The techniques investigated fall into into five major categories: 1. preirradiation device electrical tests, 2. preirradiation tests on special test devices or wafers, 3. process or design controls, 4. radiation simulation tests, and 5. radiation tests. Over 20 techniques were identified and 9 were selected for further studies.

Volume II is a summary of the test results of the verification tests performed on commercial semiconductor devices. These verification tests were performed either to supplement the limited available data for a potentially useful technique or to generate original data on previously unexamined techniques. The correlation coefficient was determined between the screening parameter and the total dose induced change in device electrical parameters on groups of 5-25 devices of a given type. No high degree of correlation was observed for any of the techniques investigated with the exception of irradiate and anneal on MOS devices.

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SECTION I
INTRODUCTION

The specific objectives of phase I of the Total Dose Hardness Assurance (HA) Program are to

(1) Identify all possible total dose HA techniques using literature, personal contacts and techniques conceived from models of basic mechanisms.

(2) Determine the effectiveness and practicability of each of the techniques using existing data, experience and analysis.

(3) Verify by experiment the effectiveness of those techniques for which an insufficient amount of data exists to reasonably establish their usefulness.

A complete discussion of the total dose HA techniques that have been identified in this program has been presented in volume I along with discussion of their effectiveness and practicality in terms of existing data, basic mechanisms models and analysis.

This report, volume II, covers the results of experiments which were performed on discrete devices in order to verify those techniques for which insufficient test data existed. The techniques which were experimentally investigated included: (1) techniques which appear promising but which had not been verified to a sufficient extent, (2) techniques which had been experimentally researched but had not been applied directly as a hardness assurance method, and (3) techniques which had been conceived from models of hole trapping or interface state generation and thus had not previously been experimentally investigated.

Because of the limitations imposed on the verification testing during phase I, several techniques which required verification testing were not investigated. This was due either to the unavailability of the appropriate test devices, e.g., gated bipolar transistors or gated diodes, or the requirement for in-process testing such as would be done on test wafers during processing. Since several of the techniques that require

some verification testing were not included in the phase I verification test program, it was decided that the verification testing would be done during the initial part of the phase II evaluation program. Therefore, this report does not address all of the verification testing that will be performed on the program but only that portion performed on "off-the-shelf" discrete MOS or bipolar components.

The basic approach to the phase I verification testing was to measure the correlation coefficient between the screening parameter and the radiation hardness of a small number of samples of a commercial device type. The number of samples ranged from 10 to 25. All irradiations were done under bias on a Co^{60} source at a fixed dose level.

A full description of the various techniques that were investigated in the phase I verification tests is given in volume I of the phase I completion report. However, a brief summary of each technique is included herein. Each section of the report, which addresses a different technique, contains, in addition to a brief description and rationale, a discussion of the approach, the samples used for the testing, the electrical tests performed, the irradiation tests, data analysis, results and suggestions for improving the technique, if applicable.

SECTION II
AVALANCHE HOLE INJECTION

1. OBJECTIVE

The objective of this experiment is to determine if a correlation exists between parameter changes resulting from avalanche hole injection and the damage produced by total ionizing dose.

2. RATIONALE

Hole trapping parameters of the oxide found by avalanching an underlying p-n junction have been investigated by Verwey (refs. 1, 2). Avalanching a p-n junction under an oxide produces holes sufficiently energetic to enter into the oxide, where they either escape to the negatively biased gate electrode or are trapped within the oxide. The altered electrical behavior of the stressed device caused by trapped positive charge yields the data required to calculate oxide trapping parameters.

An oxide with relatively few hole traps would be expected to be less susceptible to the effects of total ionizing dose. Therefore, the total number of hole traps (N_t), as determined by the avalanche injection technique, should act as a screen for parts which would show an unacceptable degradation in a total dose environment.

The original technique developed by Verwey assumes a field dependent hole current through the oxide. To determine NoS, the concentration of hole trapping centers times the capture cross section; transient picoamp hole current measurements must be made at several oxide electric field values. Complex data reduction is required, including numerical integration of measured data. Assumptions required include the diffusion length of hot holes, the interface area of the avalanching region, and uniform injection over the avalanche area.

To avoid some of the difficulties of the Verwey technique, a new technique was developed by BDM. The experimental procedure utilized is illustrated schematically in Figure 1. The p-n junction is avalanched by a fixed amount of current and the breakdown voltage immediately noted. Energetic holes attracted to the negative gate bias enter the oxide, where some are trapped. The trapped positive charge in the oxide will alter the surface potential and causes the breakdown voltage to increase. The gate bias is then made more negative to restore the initial breakdown voltage and surface potential. Under constant surface potential, the growth of the trapped oxide charge will be described as:

$$Q(t) = qN_t \ (1-\exp(-t/Tc)) \qquad \text{(Eq. 1)}$$

where N_t is the number of oxide traps, t is time, and Tc is the capture time constant. By letting time approach infinity (allowing the system to approach a static condition), $Q(t) = qN_t$ as nearly all oxide traps are filled in the region of avalanche injection. The total number of oxide traps can be calculated as:

$$N_t = \frac{\Delta V_G \ \varepsilon_{ox} \ \varepsilon_o}{q \ X} \qquad \text{(Eq. 2)}$$

where ΔV_G is the range over which the gate voltage was adjusted and X is the distance from the gate to the centroid of charge. Bakowski et al. (ref. 3) have found the traps to have characteristic distances from the semiconductor of 150-200 Å for dry oxides and about 400 Å for wet oxides. If the distance from the semiconductor to the charge centroid can be assumed to be much less than the oxide thickness, equation (2) can be approximated by:

$$N_t = \frac{\Delta V_G \ \varepsilon_{ox} \ \varepsilon_o}{q \ d_{ox}} \qquad \text{(Eq. 3)}$$

where d_{ox} is the oxide thickness.

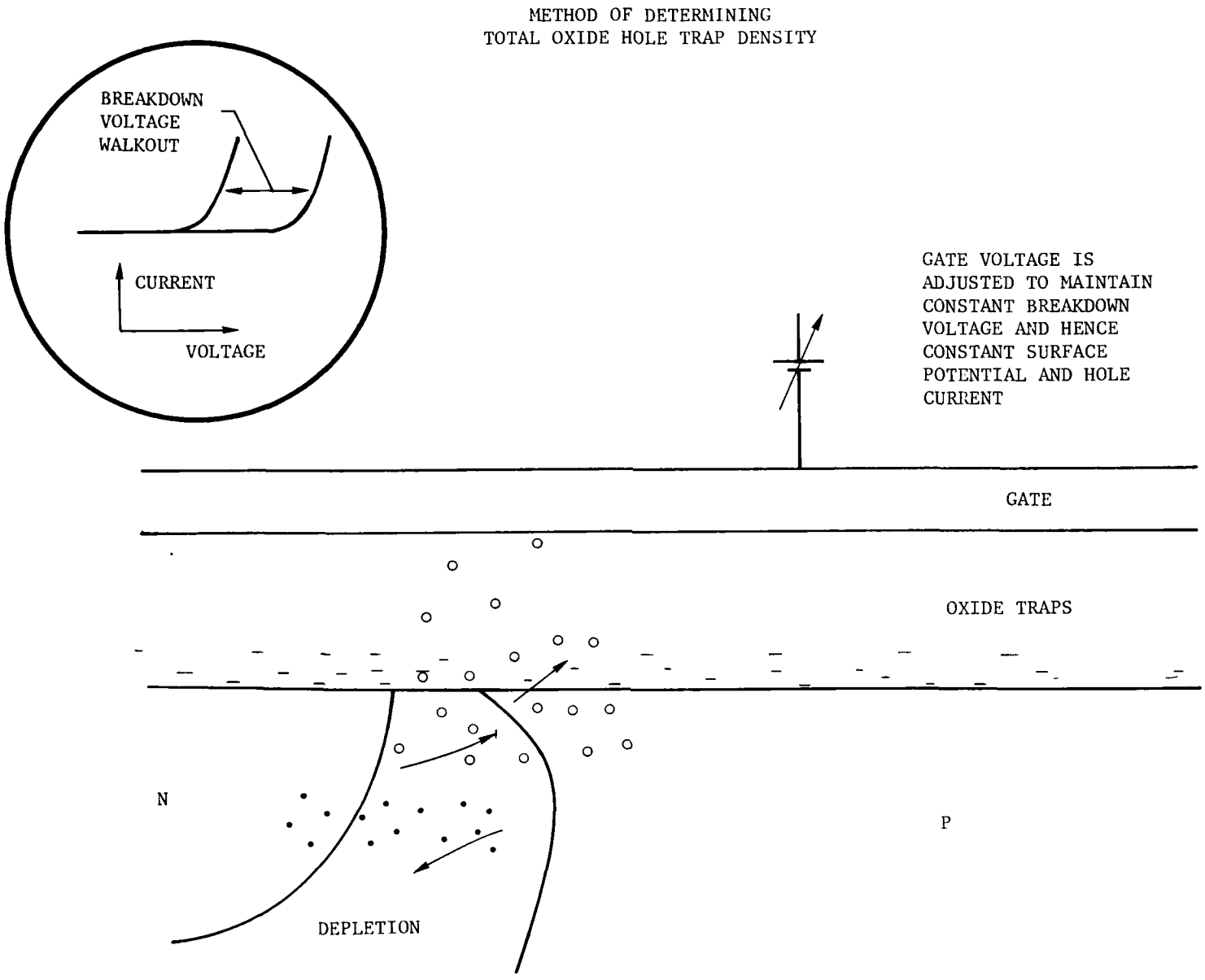

Figure 1. Method of Determining Total Oxide Hole Trap Density

Also investigated was the magnitude of the breakdown voltage increase or breakdown voltage "walkout" produced by a fixed negative gate voltage. W V_t for this condition can be obtained by reducing the p-n junction voltage to the original breakdown voltage and then decreasing the gate voltage until avalanche is initiated.

3. SAMPLES

The experimental test devices chosen where RCA 40468A MOSFETs. The 40468A is a large area N-channel depletion mode DMOS device with no gate protection. It is packaged in a TO-72 metal can. Figure 2a is a photomicrograph of the device and Figure 2b is a cross section and doping profile of the DMOS structure. Table 1 lists some of the important electrical characteristics of the device. A total of ten devices were used for the correlation studies.

4. ELECTRICAL TESTS

The threshold voltages of the test devices were determined by plotting drain current as a function of gate voltage with a drain voltage of 50mV. Threshold voltage was obtained by extrapolating along the line segment where transconductance is a maximum to the $I_D = 0$ line.

4. STRESS TESTS

The avalanche injection stress was performed on a Tektronix 577 curve tracer in the sweep mode. The breakdown voltage "walkout" or increase which can occur quite rapidly upon avalanche can be precisely monitored with the storage feature.

The source lead was stressed with a current of 100 mA with the drain floating and the substrate grounded. The initial gate bias was -10V. The source was stressed for 5 minutes. Avalanche of the drain would be impractical since the junction formed by the drain diffusion is not gated as shown in Figure 2.

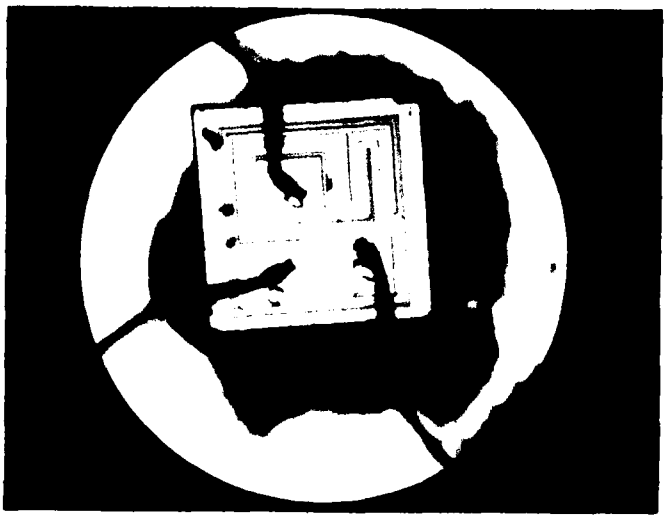

Figure 2a. Photomicrograph of the RCA 40468A (X86)

After the five minute stress, the change in gate voltage, (ΔV_G), was recorded. The gate voltage throughout the stress was constantly adjusted in a manner which kept the breakdown voltage of the source at a constant value.

In the second experiment, the source lead of undamaged samples was again stressed at 100 μA with the drain open and the substrate grounded. This time, however, the gate voltage was not adjusted but left at -10V. Stress time was 1 minute.

Under these conditions, the breakdown voltage of the source was allowed to "walkout" or increase. After stress, the gate voltage was reduced to zero volts and the voltage applied to the source was reduced to a value equal to the initial source breakdown voltage. The gate voltage was then increased slowly until breakdown was just initiated. This value was defined as the "gate recovery voltage".

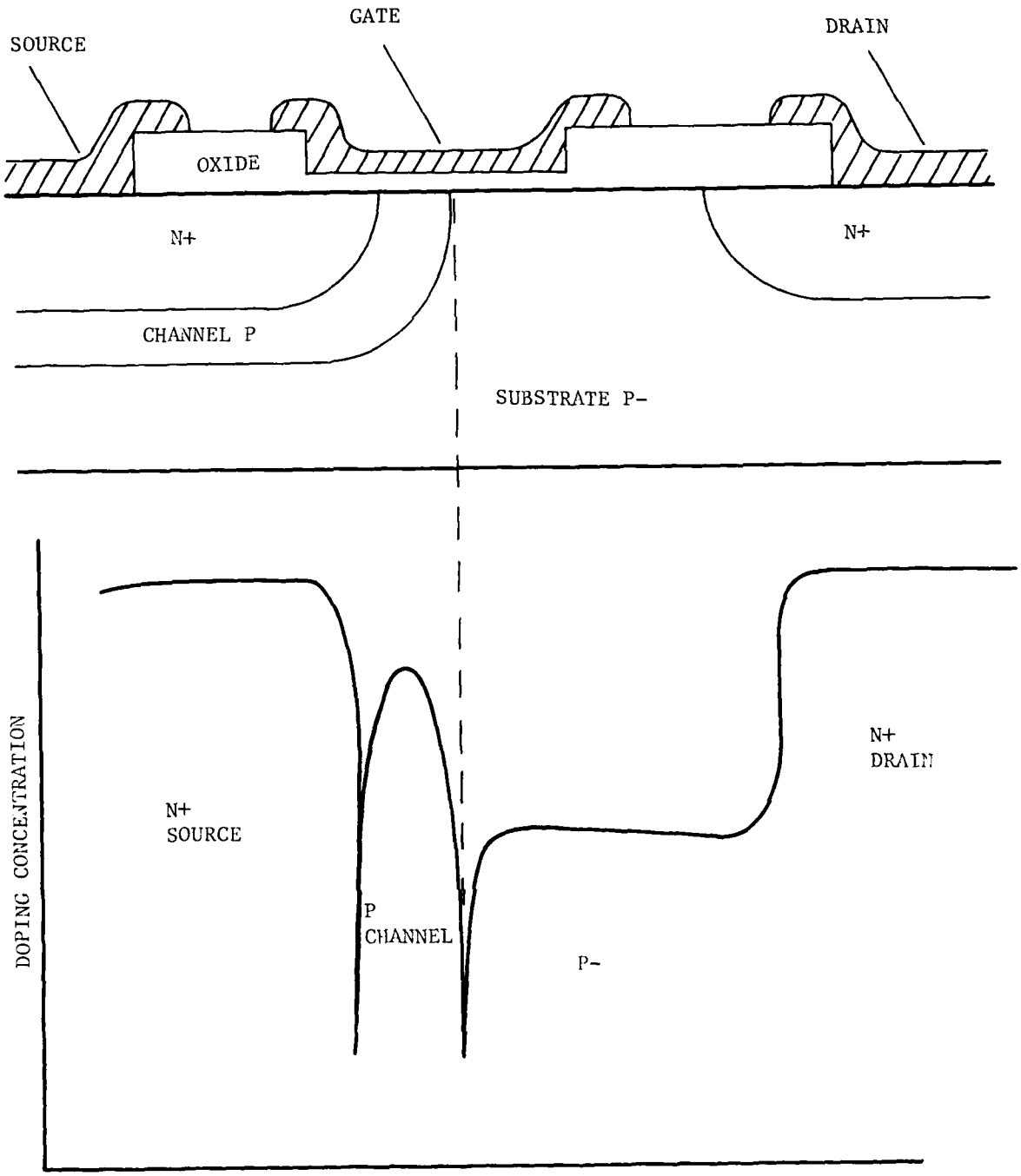

Figure 2b. Cross Section and Doping Profile of DMOS Transistor

TABLE 1. ELECTRICAL CHARACTERISTICS OF THE RCA 40468A

Characteristics	Symbols	TEST CONDITIONS						Units
		Frequency	DC Drain-to Source Voltage	DC Drain Current	Limits			
		f MHz	V_{DS} V	I_D mA	Min.	Typ.	Max.	
Drain-to-Source Cutoff Current	$I_D(off)$	-	12	V_{GS} = 8V	-	-	100	µA
Gate Leakage Current	I_{GSS}	-	0	V_{GS} = -8V	-	-	1	nA
		-	0	V_{GS} = +1V	-	-	1	nA
Zero-Bias Drain Current	I_{DSS}	-	15	V_{GS} = 0	5	15	30	mA
Small-Signal, Short-Circuit Forward Transconductance	gfs	1 KHz	15	5	-	7500	-	µmho
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15	5	-	0.25	0.35	pF
Input Capacitance	C_{iss}	1	15	5	-	5.5	-	pF
Maximum Available Power Gain	MAG	100	15	5	-	26	-	dB

6. IRRADIATION

The devices were irradiated by exposure to the AFWL 5 kilocurie Co^{60} gamma ray source. The total dose received was $5X10^5$ Rad (Si). A positive 1 volt bias was applied to the gate during the irradiation and all other leads were grounded.

7. RESULTS

Figure 3 is a plot of ΔV_G (directly proportional to N_t) as a function of the change in threshold voltage. The negative slope of the least squares fit line and poor correlation coefficient indicates that knowledge of N_t will give no indication of the magnitude of threshold voltage shift at $5X10^5$ Rad (Si).

The disappointing results can be explained by the fact that threshold voltage shift is also a function of interface state generation. Consider the "growth curves" proposed by Freeman and Holmes-Siedle (ref. 4) in Figure 4. At low doses the threshold voltage shift caused by hole capture produces a linear change in the log of ΔV_t with respect to Log of dose. At higher doses, the hole trapping saturates and the shift produced by surface states become dominant in a nonlinear manner.

The unhardened samples tested were irradiated to $5X10^5$ Rad (Si) which may be well into the trap dominated nonlinear region. If these devices were irradiated in the nonlinear region, no correlation between N_t and ΔV_t could be expected.

A further study of the work of Freeman and Holmes-Siedle indicates that avalanche hole injection may be of great use in total dose hardness assurance. Two "engineering growth curves" shown in Figures 5 and 6 are suggested as useful "for making predictions of the lifetime of MOS circuits exposed to radiation in space or laboratory environments."

The curves of Figure 5 predict that the maximum threshold shift under a negative gate bias is the gate voltage applied. This effect should be seen in the second experiment and will act as a check on the

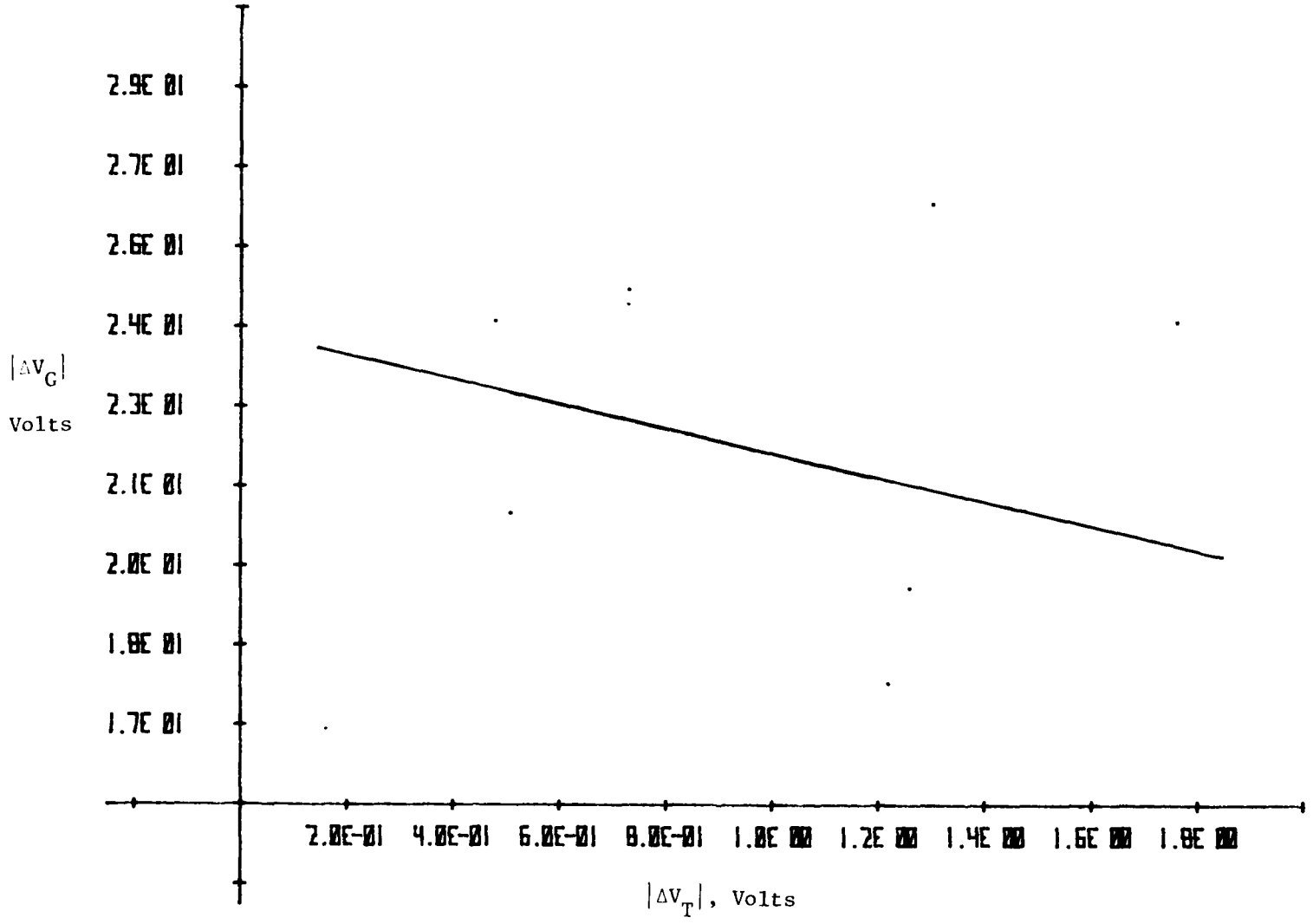

Figure 3. Change in the Gate Voltage Required to Maintain Constant Surface Potential as a Function of the Radiation Induced Threshold Voltage. R = 0.3555 ± 0.31.

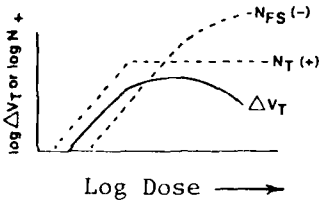

Figure 4. Typical Damage Growth Curve

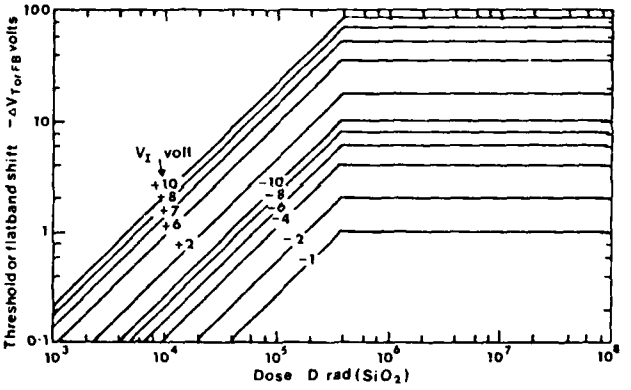

Figure 5. A set of growth curves, suitable for use by design engineers, based on a simple charge sheet buildup model. Saturation shown here is due to oxide field vanishing.

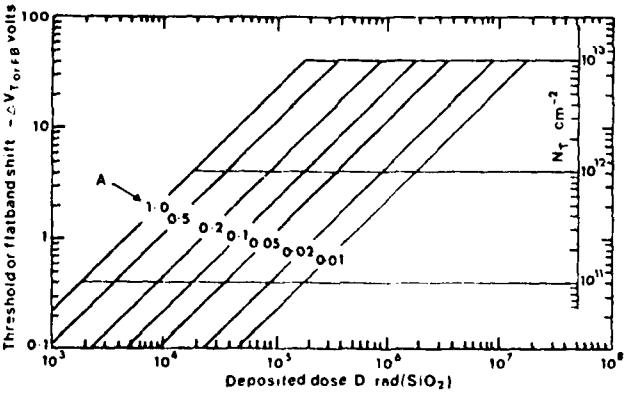

Figure 6. A set of growth curves, suitable for use by design engineers, based on a simple charge sheet buildup model. Saturation is due to trap filling.

validity of the avalanche hole injection technique. Assuming trap saturation did not occur, the "gate recovery voltage" should differ from the initial gate voltage by an amount equal to the initial gate voltage of -10 V. The average increase actually obtained was -8.5 V with a standard deviation of 1.42 V. These results indicate that the oxide charging reaches approximately 85 percent of its final value in 1 minute under the conditions stated.

It would be of value to obtain an easy method of determining both N_t and the constant "A" in Figure 6. The change in threshold voltage in terms of saturation of all available traps can be written as:

$$\Delta V_t \text{ (sat)} = \frac{q\ X}{\varepsilon_{ox}\ \varepsilon_o\ S} A \qquad \text{(Eq. 4)}$$

where X is the distance from the centroid of the charge to the gate metal (approximated by d_{ox}), A is the initial trapping probability and S is the capture cross section. For avalanche hole injection:

$$\Delta V_t \text{ (sat)} = \Delta V_G \qquad \text{(Eq. 5)}$$

Taking the typical value of S as $5X10^{-14}$ cm^2, the "A" value for the oxide can be calculated as:

$$A = \frac{\Delta V_G\ \varepsilon_{ox}\ \varepsilon_o\ (5X10^{-14}\ cm^2)}{q\ X} \qquad \text{(Eq. 6)}$$

where X may be approximated by d_{ox} in some cases.

A typical ΔV_G obtained with the test devices was 20 V. Assuming d_{ox} = 0.1 μm:

$$A = \frac{(30\ V)\ (3.9)\ (8.854X10^{-12}\ Fm^{-1})\ (5X10^{-18}\ M^2)}{(1.602X10^{-19}\ coulomb)\ (0.1X10^{-6})} \qquad \text{(Eq. 7)}$$

$$A = 0.215$$

which is the A value for a moderately soft oxide. The total number of oxide traps is estimated as:

$$N_t = \frac{(20\ V)\ (3.9)\ (8.854X10^{-12}\ Fm^{-1})}{(1.602X10^{-19}\ coulomb)\ (0.1X10^{-6}m)} \qquad \text{(Eq. 8)}$$

$$N_t = 4.31\ X10^{12}\ traps/cm^2$$

which is consistent with the known properties of oxides.

8. IMPROVEMENTS

A decisive verification of avalanche hole injection will require tests on known hard and soft oxides. The variation in hardness of a sample of commercial parts may be too small for the avalanche hole technique to resolve.

The test parts should be irradiated at low doses to avoid the effects of surface states. When used as a screen, surface state effects will have to be factored in separately.

It is possible to improve the avalanche hole injection technique. If the small oxide current could be successfully measured, it would be possible to estimate the capture cross section of the hole traps.

Maier* has suggested that the surface states produced by avalanche hole injection may be measured by noting the increase in the junction leakage current produced by the stress. A gated diode can be used to make this measurement by depleting the surface under the gate and noting

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*Private Communication with Roe Maier of AFWL.

the increase in leakage current. No such increase was observed when attempting to use the 40468A as a gated diode. The observed leakage current (nanoamps) is probably due to package leakage and bulk recombination currents which are much larger in magnitude than the surface generation current component.

It is suggested that in phase II, the p-n junction avalanche technique be applied to a gated diode, for which both the ΔV_G to maintain a constant breakdown voltage and the increase in surface recombination velocity, ΔI_{SO}, can be monitored as a function of stress.

In conclusion, the avalanche hole injection technique has not been verified as a functional screen for parts to be subjected to a total dose environment. However, reasons have been given why these results should not be considered conclusive. Values of the total number of traps and the initial trapping probability were calculated for a typical test device which are consistent with the known properties of gate oxides. The computed oxide parameters predict that the RCA 40468A possesses a moderately soft oxide.

The avalanche hole injection technique may still prove to be a valid simulation of the radiation environment if applied to a gated diode structure and evaluated over a range of stress conditions and radiation levels.

SECTION III
NEGATIVE BIAS TEMPERATURE STRESS (NBT)

1. OBJECTIVE

The purpose of the NBT experiment is to determine the degree of correlation between damage produced by NBT and damage produced by total ionizing dose.

2. RATIONALE

Several studies (refs. 5, 6) have investigated the effects of heating MOS devices with a negative bias applied to the gate. The investigators found that NBT treatment increased the surface state density and the density of positive charge. Jeppson and Svensson (ref. 7) suggest that at low electric fields, stress activates a chemical reaction which produces a positive oxide charge and a surface defect, while at high electric fields, holes are injected from the semiconductor and the trapped holes create surface states.

Because NBT and total dose both produce similar damage, i.e., trapped holes and interface states, NBT stress may act as a substitute for radiation tests. Such a substitution, if possible, could save significant amounts of time and expense by eliminating the need for radiation testing, except perhaps on a periodic basis.

3. JUSTIFICATION

NBT is not the only possible "radiation simulator" technique possible. Hole injection by p-n junction avalanche (discussed previously) is a room temperature technique but produces such a narrow region of damage that device electrical characteristics are virtually unaffected. Bulk avalanch-

ing techniques can also be done at room temperature but only with complex equipment on a specially fabricated test structure. NBT, while requiring high temperatures, is simple and can be performed on any gated device which has no input protection network.

4. PROCEDURE

The experimental procedure chosen was to subject N-channel MOSFETs to a low-field NBT treatment. The first group of samples were stressed at 300¼C for 15 minutes with a gate bias of -20 volts and all other leads grounded. The damage was then annealed out at 300¼C for 1 hour with all leads shorted. The devices were then irradiated under bias 1 X 10^6 Rad (Si) by exposure to Co^{60}. The correlation between the change in threshold voltage induced by NBT and the change in threshold voltage produced by the irradiation was determined.

5. SAMPLES

RCA 40468A MOSFETs were used as test vehicles in the experiment. The 40468A is an N-channel depletion mode DMOS device which has no gate protection network.

6. ELECTRICAL TESTS

Threshold voltage for the samples was determined by plotting the drain current versus gate voltage with a drain voltage of 50 mV. Threshold voltage was obtined by extrapolating along the line segment where transconductance is a maximum to the $I_D = 0$ line. The slope of the straight line segment is directly proportional to the maximum field effect mobility.

7. IRRADIATION

Devices were irradiated on the AFWL 5 kilocurie Co^{60} gamma ray source. A gate bias of +1V was applied during the irradiation and all other leads were grounded.

8. DATA ANALYSIS

Figure 7 is a plot of the change in threshold voltage due to radiation (ΔV_{TR}) as a function of the change in threshold voltage caused by NBT (ΔV_{TS}). A least squares fit is drawn through the data. The correlation coefficient is 0.83 ± 0.14. Relevant statistics for this test are given in Table 2.

Table 2

TEST RESULTS

	Prestress $\lvert V_T \rvert$	$\lvert \Delta V_T \rvert$ NBT	V_T(Prestress)/V_T(Anneal)	$\lvert \Delta V_T \rvert$ RAD
$\bar{X}$	1.46 V	0.18 V	0.97	2.11 V
σ	0.086	0.19	0.078	0.61
n	10	7	7	7

Encouraged by these results, the experiment was repeated for an additional 15 test devices with some variations intended to improve the correlation. The NBT stress time was doubled to 30 minutes to attempt to produce a more substantial level of damage. More points were measured on the drain current versus gate voltage characteristic curves so $\lvert V_T \rvert$ could be measured with greater accuracy. The anneal bake was lengthened to 6 hours in an attempt to make the ratio [Prestress $\lvert V_T \rvert$/Anneal $\lvert V_T \rvert$] more closely approach unity. The radiation level was reduced to $1X10^5$ Rad (Si) so that the change in threshold voltage produced by irradiation would be comparable to the change caused by NBT. The statistical results of this experiment are given in Table 3 (m = transconductance).

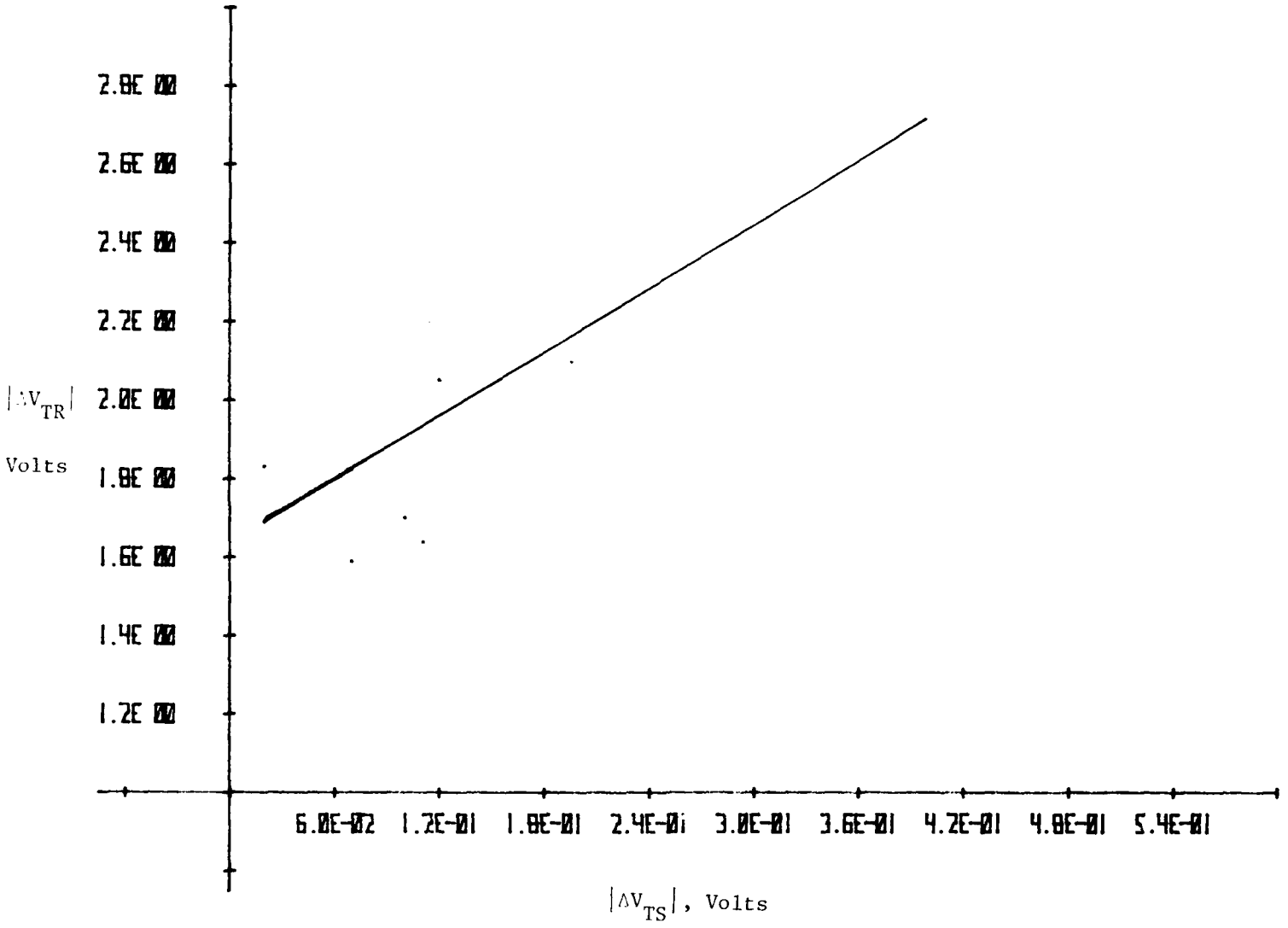


Figure 7. Radiation Induced Change in Threshold Voltage as a Function of the Stressed Induced Change in Threshold Voltage. R = 0.83 ± 0.14

TABLE 3. TEST RESULTS

	Initial		NBT		Anneal		Radiation	
	$\lvert V_T \rvert$	$\lvert m \rvert$	$\lvert \Delta V_T \rvert$	$\lvert \Delta m \rvert$	$\lvert V_T(\text{Initial})/V_T(\text{Anneal}) \rvert$	$\lvert m(\text{Initial})/m(\text{Anneal}) \rvert$	$\lvert \Delta V_T \rvert$	$\lvert \Delta m \rvert$
n	15		15		15		15	
$\bar{X}$	1.47 V	250.13 µmho	0.137 V	67.33 µmho	0.984	1.04	1.27 V	142.33 µmho
Max	1.77	315	0.27	175	1.007	1.17	1.52	167
Min	1.38	167	0.06	-15	0.953	0.75	1.04	34
σ	0.10	45.68	0.049	48.91	0.015	0.10	0.130	31.6

The ratio of $|V_T|$ initial to $|V_T|$ anneal for the 1 hour anneal was 0.97 with a standard deviation of 0.078. The annealing ratio for the 6-hour anneal was 0.984 with a standard deviation of 0.015, indicating that a 6-hour 300°C bake produced better anneals than the 1-hour bake.

A plot of $|V_T(\text{initial})-V_T\ (\text{NBT})|$ as a function of $|V_T(\text{anneal})-V_T\ (\text{Rad})|$ is shown in Figure 8. The correlation coefficient between the two parameters was found to be -0.30 ± 0.25.

Because of the relatively large degradation in the field effect mobility produced by both NBT and radiation, this parameter was also studied. Figure 9 is a plot of the change in maximum transconductance produced by NBT as a function of the change in maximum transconductance produced by radiation. The correlation coefficient is -0.12 ± 0.27.

9. DISCUSSION

The correlations obtained for the more tightly controlled experiment are discouraging. However, explanations for these results suggest NBT may yet prove useful.

The large changes in transconductance suggest that surface state creation is dominating the radiation response. Surface state domination can produce threshold voltage shift turnabout, as illustrated by Figure 10. If NBT produces damage equivalent to dose X_1 of Figure 10 and the irradiation level is at dose level X_2, the nonlinear characteristic will reduce the correlation between NBT and radiation.

Other factors may also be responsible for the poor correlations obtained. NBT causes a hole flux to flow from the semiconductor toward the metal while the positive voltage applied during irradiation produced a hole flux in the opposite direction. Except for the case of hole trap saturation, the two fluxes should produce slightly different charge centroids. Negative gate biases also have a characteristic saturated threshold voltage different than that of positive gate biases. This saturated threshold voltage occurs when compensating charges built up

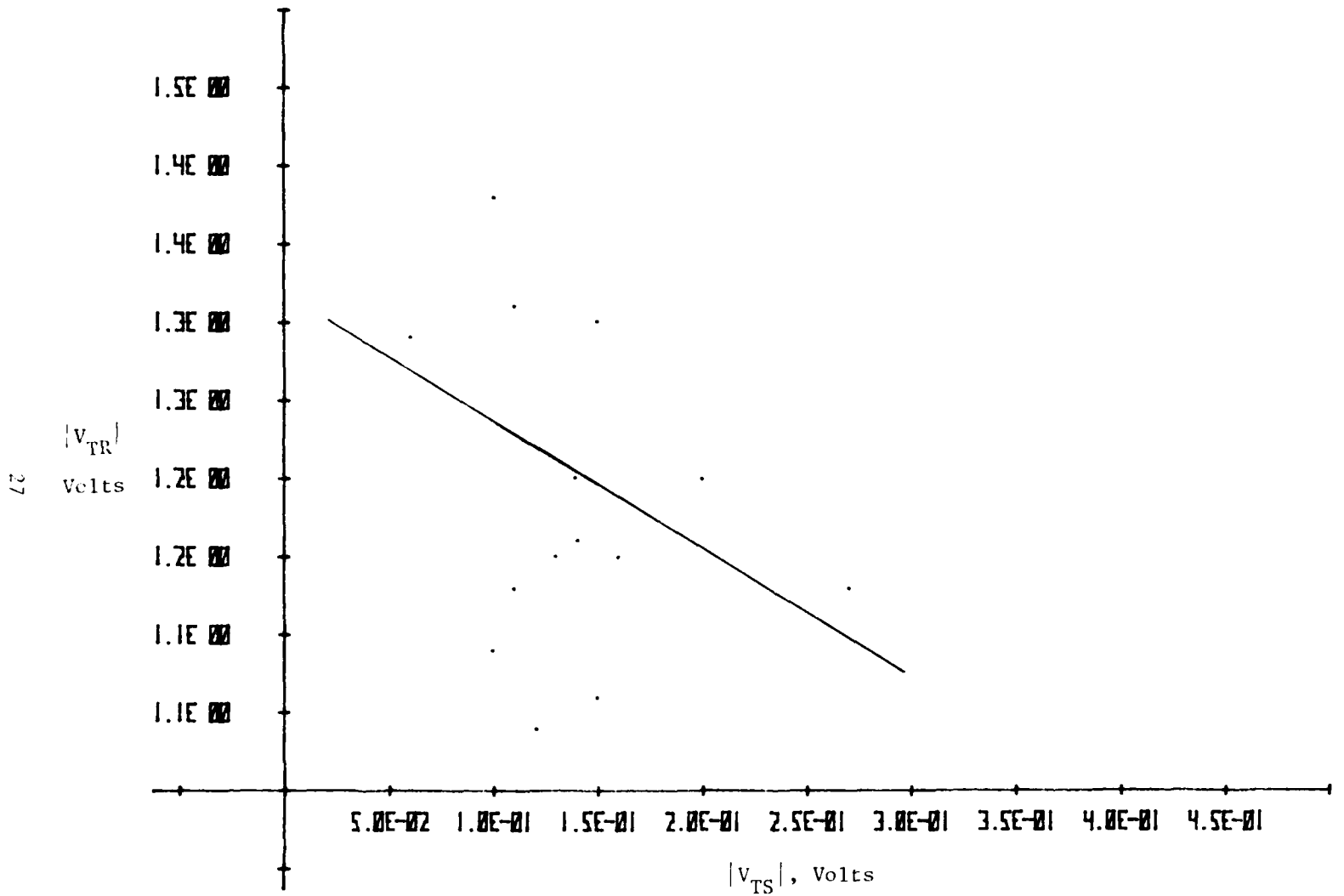


Figure 8. Change in Threshold Voltage Produced by Stress as a Function of Stress Induced Threshold Voltage Change R = -0.304

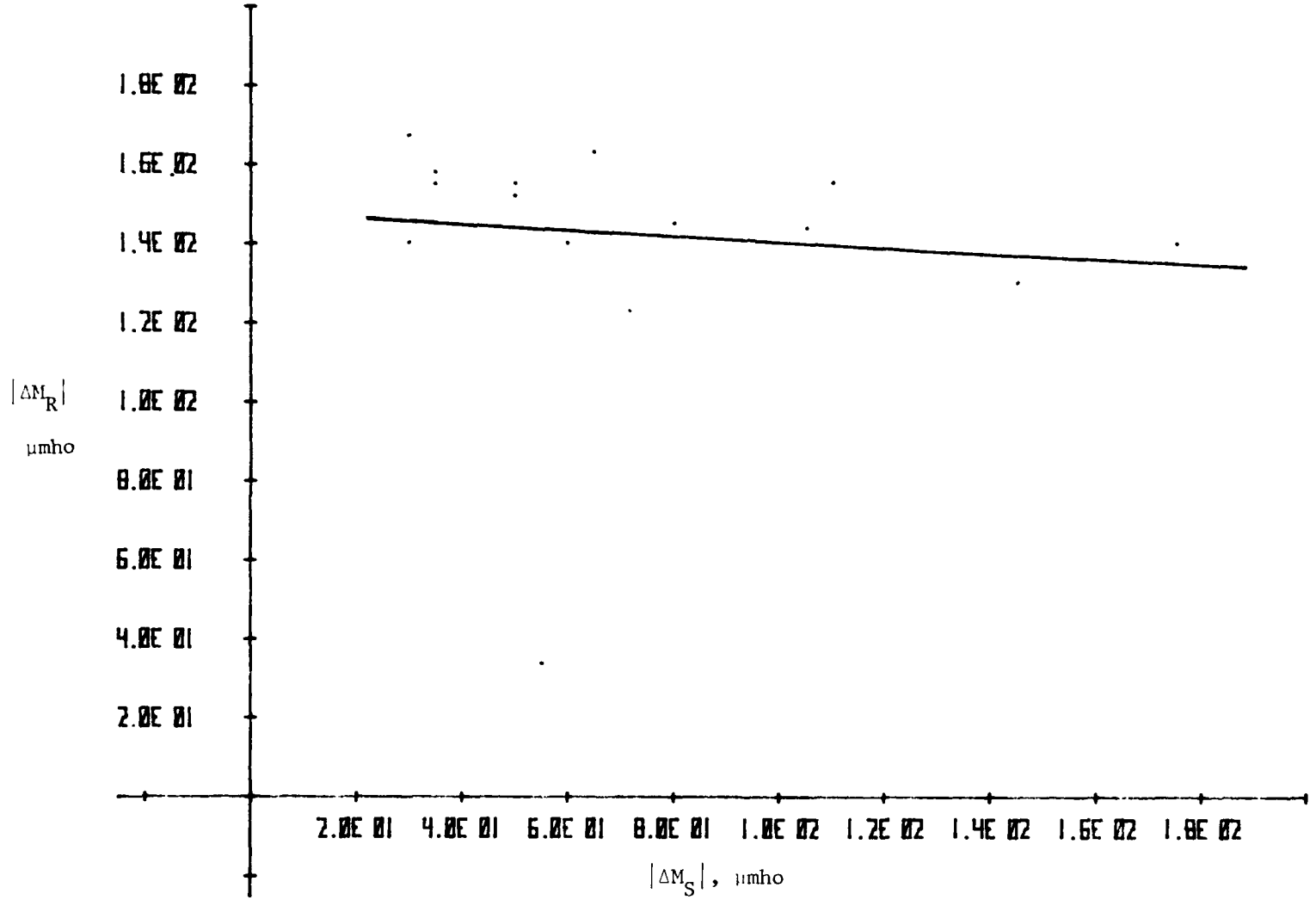


Figure 9. Radiation Induced Change in Transconductance as a Function of the Stress Induced Changed in Transconductance. R = -0.121 ± 0.27

in the oxide cause the electric field to vanish. In addition, the high temperatures utilized for NBT may alter the physical constants and dynamics of the trapping process. Finally, it has not been established whether the high field or low field regime is the more suitable of radiation. NBT effects will occur over a wide range of temperatures and electric fields.

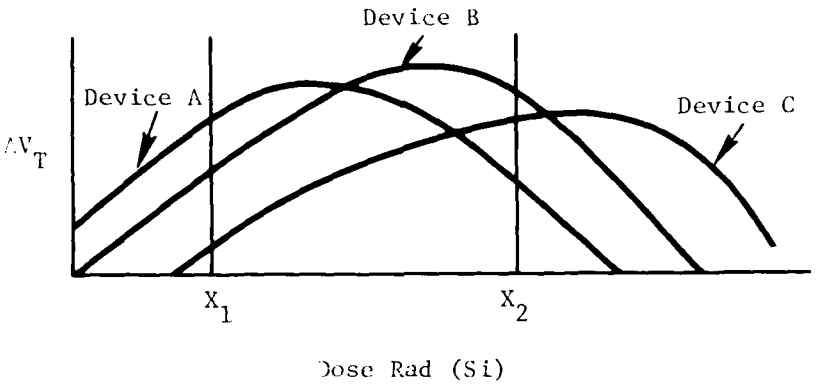


Figure 10. Turnabout Produced by Surface States

10. IMPROVEMENTS

In the hase II verification tests for NBT, ΔV_T versus stress time will be performed at both high and low electric field strengths. These will be compared to the "growth" curves for ΔV_T vs γ. In addition, p-channel devices will be investigated. Tests will also be performed on p and n substrate MOS capacitors to determine if the capacitor structure may prove a better test vehicle for this technique.

SECTION IV

H_{FE} DEGRADATION FROM EMITTER - BASE (E-B) STRESS

1. OBJECTIVE

The purpose of this experiment is to determine if gain degradation produced by E-B stress is correlated to gain degradation produced by total ionizing dose.

2. RATIONALE

Several studies (refs. 8, 9, 10) have shown that avalanche breakdown of the base-emitter junction in bipolar transistors produces energetic holes which may be injected into the base oxide, producing surface damage similar to the damage produced by ionizing radiation. Hole injection produces an increase in the density of surface states in the base, which act as recombination centers, and positive oxide charges, which alter the surface potential. Current gain degradation is the major effect produced in transistors after accumulation of a total ionizing dose.

Transistor susceptibility to gain degradation produced by total ionizing dose should be related to the gain degradation produced by E-B stress, if the hole injection process can be controlled by a gate electrode over the base oxide. In the absence of a gated base, injection may still occur but will be controlled by the naturally occurring surface fields, whose magnitudes are not known.

3. JUSTIFICATION

Because gated devices were not available for the verification phase, E-B stress was applied to commercial bipolar transistors to determine if the natural surface fields would produce a controlled injection and allow E-B stress to be used as a sample part screen for commercial packaged devices.

4. PROCEDURE

For the experimental test procedure, a sample of packaged transistors was chosen as test structures. These transistors were then subjected to the following procedures:

(1) Pretest Electrical Characterization
(2) Stabilization Bake at 280°C for 10 minutes
(3) Poststabilization Electrical Characterization
(4) Emitter-Base Stress
(5) Poststress Electrical Characterization
(6) Anneal Bake for 6 Hours at 275°C
(7) Postanneal Electrical Characterization
(8) Gamma Irradiation to $0.5X10^6$ Rad (Si)
(9) Postradiation Electrical Characterization

The purpose of the device stabilization was to ensure that changes which occurred during the high temperature bake were due only to the damage annealed out during the stress step. The poststabilization and postanneal characteristics serve as baselines which are nearly equal for measuring damage produced by stress and radiation.

5. SAMPLES

Forty transistors of 4 device types were tested in this verification test. The transistors included 10-2N2720 NPN low power, 10-2N2944 PNP low power, 10-2N3468 PNP high power and 10-2N2537 NPN switching transistors. All transistors were encapsulated in metal packages.

6. ELECTRICAL TESTS

Recombination centers introduced into the base region will not alter the injection of minority carriers into the base region and thus will have no effect on collector current. However, the recombination of minority

carriers in the base will result in an increase in base current. This additional base current component is especially important at low collector currents where surface recombination can become the dominant factor determining current gain. Therefore, base current at a constant value of collector current was determined at each electrical characterization step. The values of collector current at which base current was measured were 10 μA, 100 μA, 1 mA, and 10 mA. Measurements were made on a Tektronix 577 curve tracer with a collector to emitter voltage of 6.5 volts.

All devices except the 2N2944 were stressed for 1 minute by avalanching the base-emitter junction at 10 mA and leaving the collector open. The 2N2944 was stressed at 1 mA for 1 minute to keep the power dissipation caused by the high base-emitter breakdown voltage at acceptable levels.

7. IRRADIATION

The test devices were irradiated by exposure to the AFWL 5 kilocurie Co^{60} gamma ray source. The test devices were irradiated to a total ionizing dose of $5X10^5$ Rad (Si). All devices were irradiated with a collector-base reverse bias of 10 volts. The base and emitter leads were grounded.

8. RESULTS

A summary of device behavior throughout the test sequence will be given in terms of the base current required to maintain a collector current of 100 μA.

The stabilization bake caused the base current of some devices to increase while other devices showed a decrease. A summary of device behavior following the bake is shown in Table 4. $\bar{I}_B$ is the post-bake average base current. F_{INC} is defined as:

$$\frac{I_B \text{ (Stabilization)}}{I_B \text{ (Initial)}} \qquad \text{(Eq. 9)}$$

for the device which produces the largest quotient. F_{DEC} also uses equation 9, but this number is for the device with the smallest quotient.

Table 4

EFFECT OF STABILIZATION

Device	$\bar{I}_B$	F_{INC}	F_{DEC}
2N2720	268 nA	1.03	0.92
2N2944	351 nA	1.06	0.99
2N3468	2.59 μA	1.01	0.93
2N2537	5.89 μA	1.85	0.77

Similar results for the base current following stress are shown in Table 5. F^S_{INC} is defined as:

$$\frac{I_B \text{ (Stress)}}{I_B \text{ (Stabilization)}} \qquad \text{(Eq. 10)}$$

for the device which produces the largest value. F^S_{DEC} describes the device with the smallest change.

Table 5

EFFECT OF STRESS

Device	I_B	F^S_{INC}	F^S_{DEC}
2N2720NPN	552 nA	2.96	No decrease observed
2N2944PNP	481 nA	2.30	No decrease observed
2N3468PNP	2.69 μA	1.09	0.995
2N2537NPN	3.20 μA	1.91	0.49

The surprising result of Table 5 is that stress can produce an increase in current gain. This anomalous gain increase has been attributed to injected positive charge bringing the silicon surface in the base region out of depletion, where maximum recombination occurs.

The purpose of the annealing step was to bring the electrical characteristic back to the poststabilization values. Table 6 is a summary of the annealing results. $\Delta\bar{I}_B$ of Table 6 is equal to the post anneal average base current minus the poststabilization average base current. F^A_{INC} and F^A_{DEC} are the largest and smallest values of:

$$\frac{I_B \text{ (Anneal)}}{I_B \text{ (Stabilization)}} \qquad \text{(Eq. 11)}$$

Table 6

ANNEAL RESULTS

Device	$\bar{I}_B$	ΔI_B	F^A_{INC}	F^A_{DEC}
2N2720	305 nA	38 nA	1.30	None*
2N2944	385 nA	34 nA	1.16	None
2N3468	2.78 μA	0.19 μA	1.14	None
2N2537	6.12 μA	0.23 μA	1.19	0.93

*None - No device had an $\frac{I_B \text{ (Anneal)}}{I_B \text{ (Stabilization)}} < 1$

Table 6 indicates that, in almost all cases, the stress damaged transistors cannot recover to their prestress current gain values by applications of an anneal cycle. However, annealing did reduce damage significantly.

To be effective as a screen, the level of damage produced by stress should correlate with the damage caused by the radiation exposure. Figures 11a-d are plots of the change in one over gain between the stabilized parts and the stressed parts, as a function of the change in one over gain between the annealed parts and the irradiated parts for each device type.

Figure 11a, the plot of $\Delta 1/\beta_s$ as a function of $\Delta 1/\beta_\gamma$ for the 2N3468, produces a least squares fit to the data with a correlation coefficient of -0.11 ± 0.35, or no correlation at all. Figure 11b shows a correlation coefficient between stress and radiation damage of 0.64 ± 0.21. Gross features of Figure 11b, however, are discouraging. One device which showed the next to the lowest change of stress induced damage showed the highest level of radiation induced damage. Figure 11c produced a correlation coefficient of -0.64 ± 0.21 which opposes the model these tests are designed to support. Figure 11d gives no indication that the devices with the highest stress induced damage show high levels of radiation induced damage.

9. CONCLUSIONS

It is obvious that the emitter-base stress test as conducted is unsuitable as a screen. However, this result is not totally unexpected because of the inability to control the hole injection without a gated base region. With a base electrode, greater control of the hole injection would be possible. In addition, a base current versus gate voltage curve could be generated which would allow the effects of positive charges in the base oxide to be predicted.

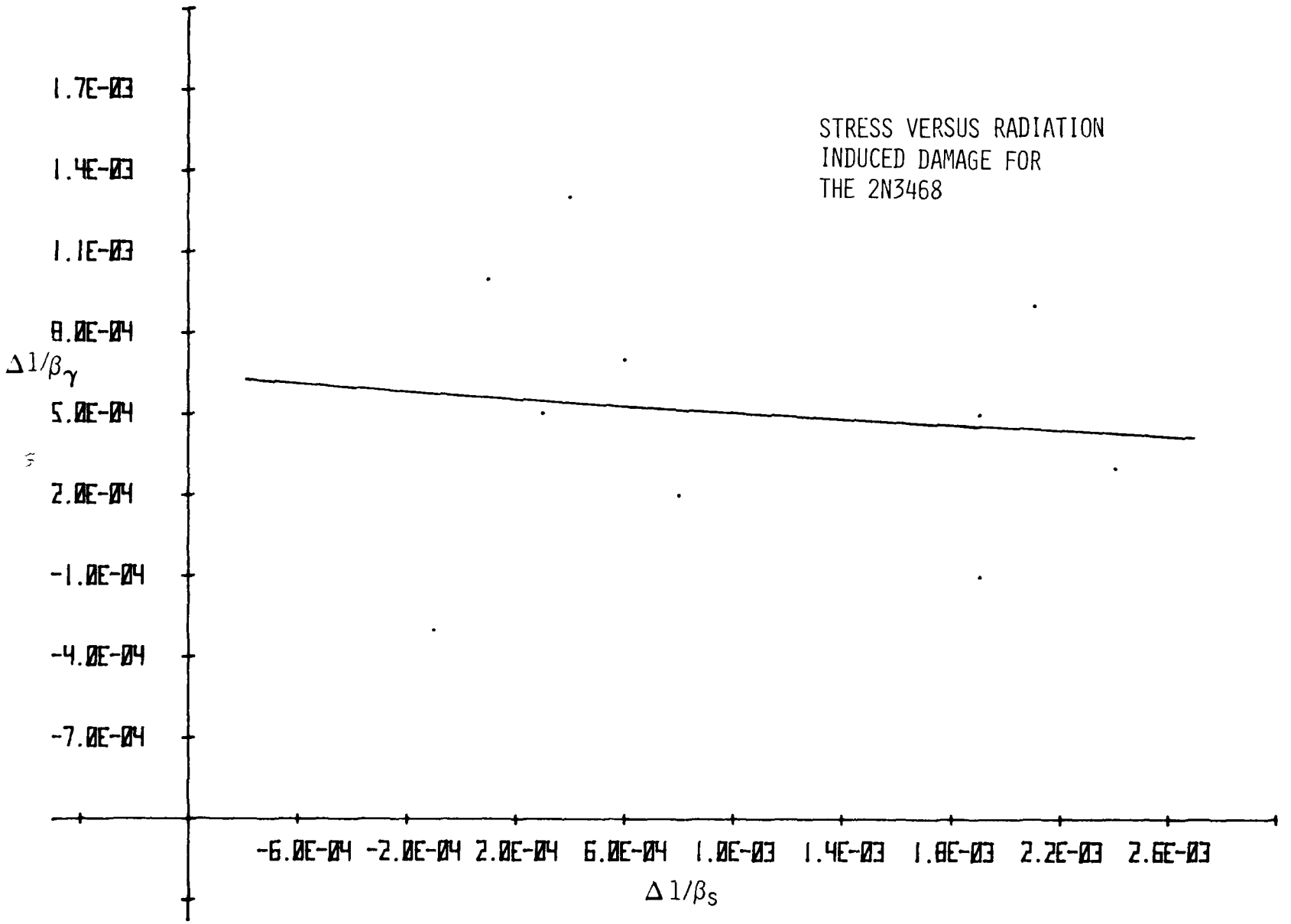


Figure 11a. Stress Versus Radiation Induced Damage for 2N3468. R = 0.11 ± 0.35

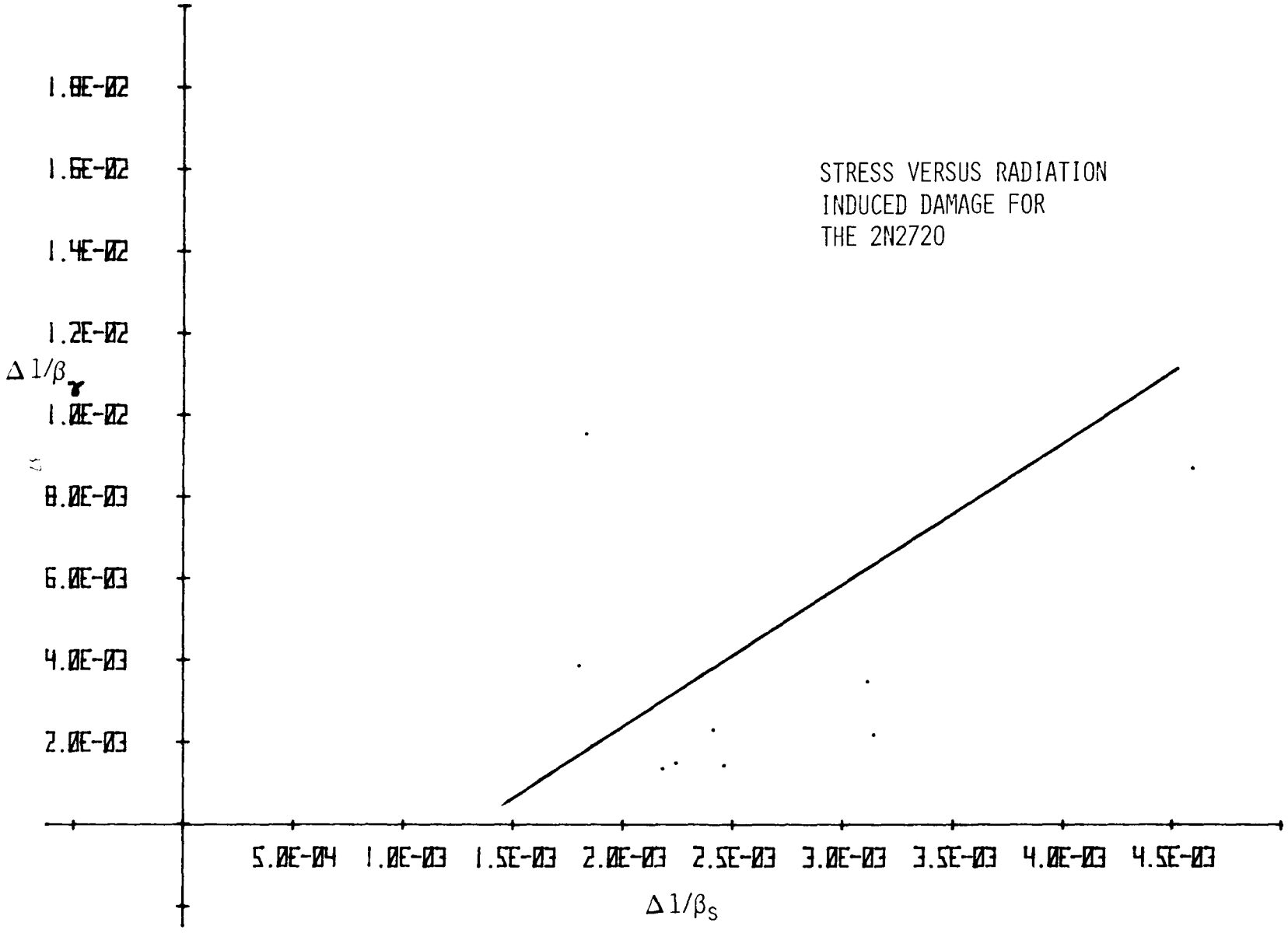


Figure 11b. Stress Versus Radiation Induced Damage for the 2N2720. R = 0.64 ± 0.21

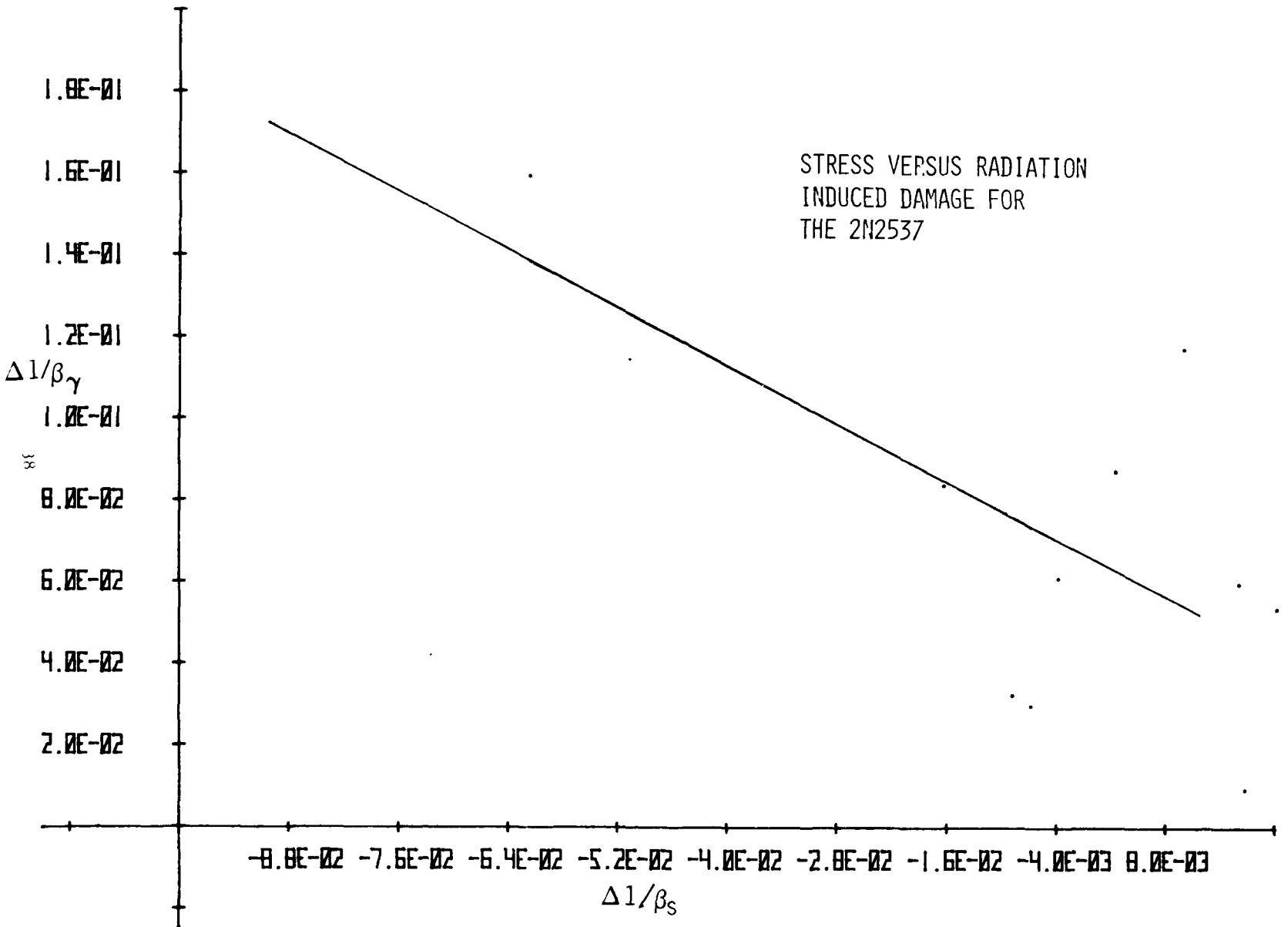


Figure 11c. Stress Versus Radiation Induced Damage for the 2N2537. R = -0.64 ± 0.21

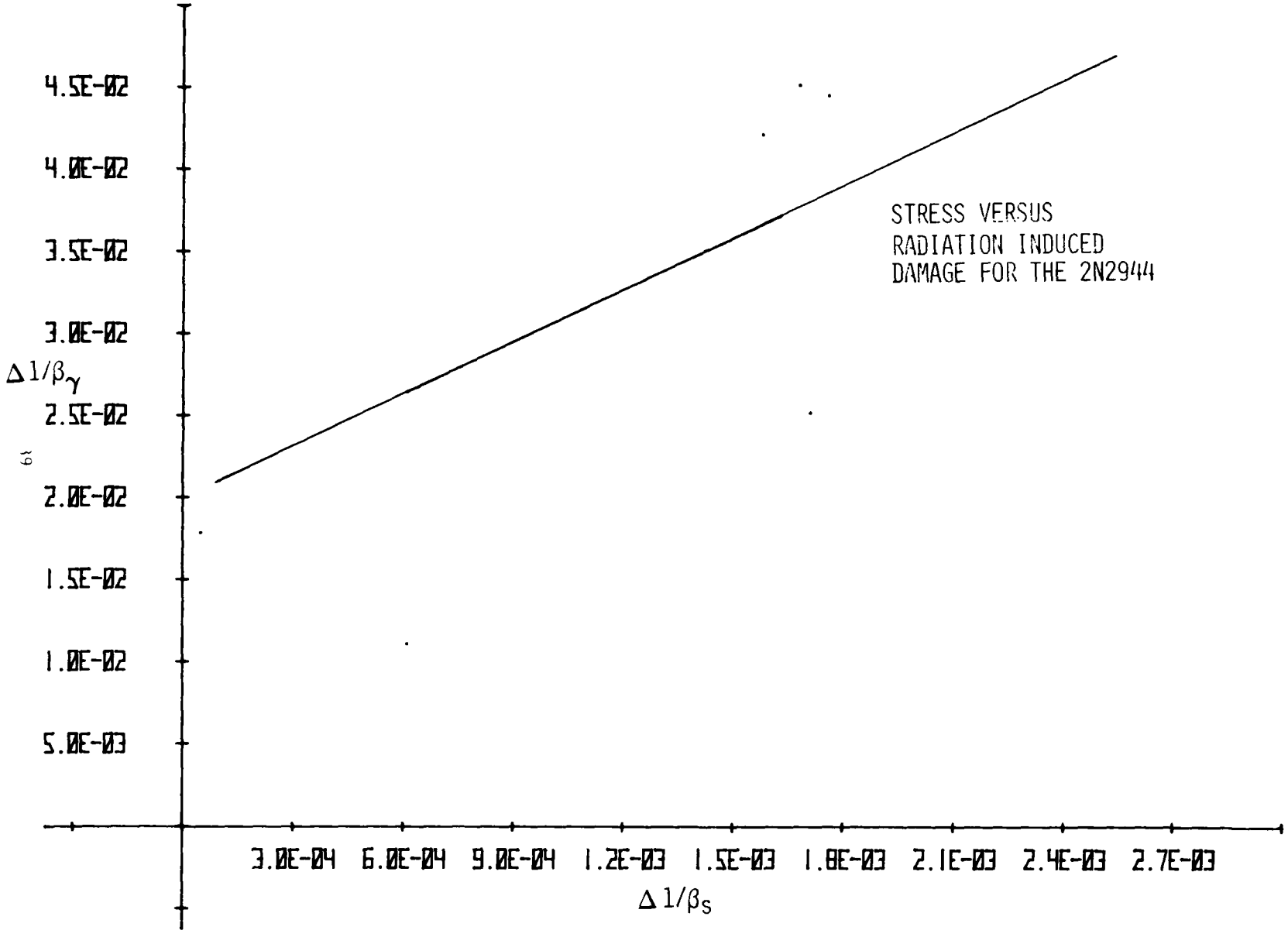


Figure 11d. Stress Versus Radiation Induced Damage for the 2N2944. R = 0.62 ± 0.22

SECTION V
EDGE STATES BY NOISE MEASUREMENTS

1. OBJECTIVE

The purpose of this experiment was to determine if a correlation exists between the density of edge states near the band edge and the radiation susceptibility of a device to total ionizing dose. Surface states density was inferred from measurements of electrical noise.

2. RATIONALE

Evidence has been presented by Pepper (refs. 11, 12) that the oxide hole trap consists of a dipole charge near the oxide-semiconductor interface in the oxide layer. Because of the weak field of dipoles, they would be expected to produce interface states with very shallow levels.

Sah and Hielscher (ref. 13) found that the square of the low frequency electrical noise at the gate of an MOS structure is directly proportional to the density of surface states with energies at the Fermi level. By adjusting the Fermi level close to the band edge, the shallow energy states produced by dipoles may become the dominant noise voltage term. The square of the noise voltage would then be related to the number of oxide hole traps.

3. JUSTIFICATION

Other methods of surface state measurement were considered but rejected. The C-V method was rejected because it must be performed at the wafer probe level and it is only accurate in the midgap region. The method utilized by Pepper of measuring the effect of substrate bias on

conductivity was considered impractical because temperatures of 4.2°K were required. Hall effect measurements required special test structures and equipment.

The advantage of noise measurements is that they can be made using commercial equipment. Also, measurements can be made in inversion on packaged MOSFETs.

4. PROCEDURE

The procedure used to measure edge states was to measure the equivalent gate noise of MOS transistors in strong inversion. In strong inversion, the Fermi level can be expected to be within a few tenths of an eV of the band edge. Any voltage drop across the channel should be minimized so the Fermi level will be uniformly constant within the device. The noise measurement must be made at a low frequency (< 20 Hz) to insure detection of states with slower time constants. Following irradiation of the test devices, the square of the low frequency noise can be compared to the change in threshold voltage produced by the radiation.

5. SAMPLES

The test samples used in this experiment were RCA 40468A MOS transistors. These devices are N-channel depletion mode DMOS with no gate protection.

6. ELECTRICAL TESTS

Low frequency gate noise of the test samples was measured using a HP4470A Transistor Noise Analyzer. The 4470A was utilized because it is one of the few commercial instruments suitable for measuring MOSFET noise. Systems such as the one used by Sah (ref. 13), which can make measurements across the band gap, were not fabricated due to program constraints.

The drain voltage was maintained at the smallest possible value (68 mV) that the HP4470A would allow. Drain current was set to 100 μA. The equivalent RMS gate voltage at 10 Hz at a bandwidth of 1 Hz was read directly from a panel meter.

The threshold voltage of the test devices were measured in the linear region by plotting drain current as a function of gate voltage with a drain voltage of 50 mV. $|V_T|$ was obtained by extrapolating along the line segment where transconductance is a maximum to the $I_D = 0$ line.

7. IRRADIATION

The devices were irradiated by exposure to the AFWL 5 kilocurie Co^{60} source. The total dose received was $1X10^6$ Rad (Si). The gates were biased at +1V during the irradiation and all other leads were grounded.

8. RESULTS

The squared noise voltage plotted as a function of change in threshold voltage is shown in Figure 12.

The correlation coefficient of 0.22 ± 0.34 and features of the plot indicate that low frequency gate noise will not predict threshold voltage shift of MOSFETs at a dose level of $1X10^6$ Rad (Si).

9. ANALYSIS

There are several reasons for the poor results. If the $(noise)^2$ measured was proportional to the dipole density, a poor correlation could result due to the nonlinear damage characteristic observed at the higher doses. To be conclusively tested for value as a screen, the test samples would have to include hard and soft oxides, with irradiation levels kept low.

The most likely explanation for the poor correlation is that the electrical noise observed was not from dipole charges but from other

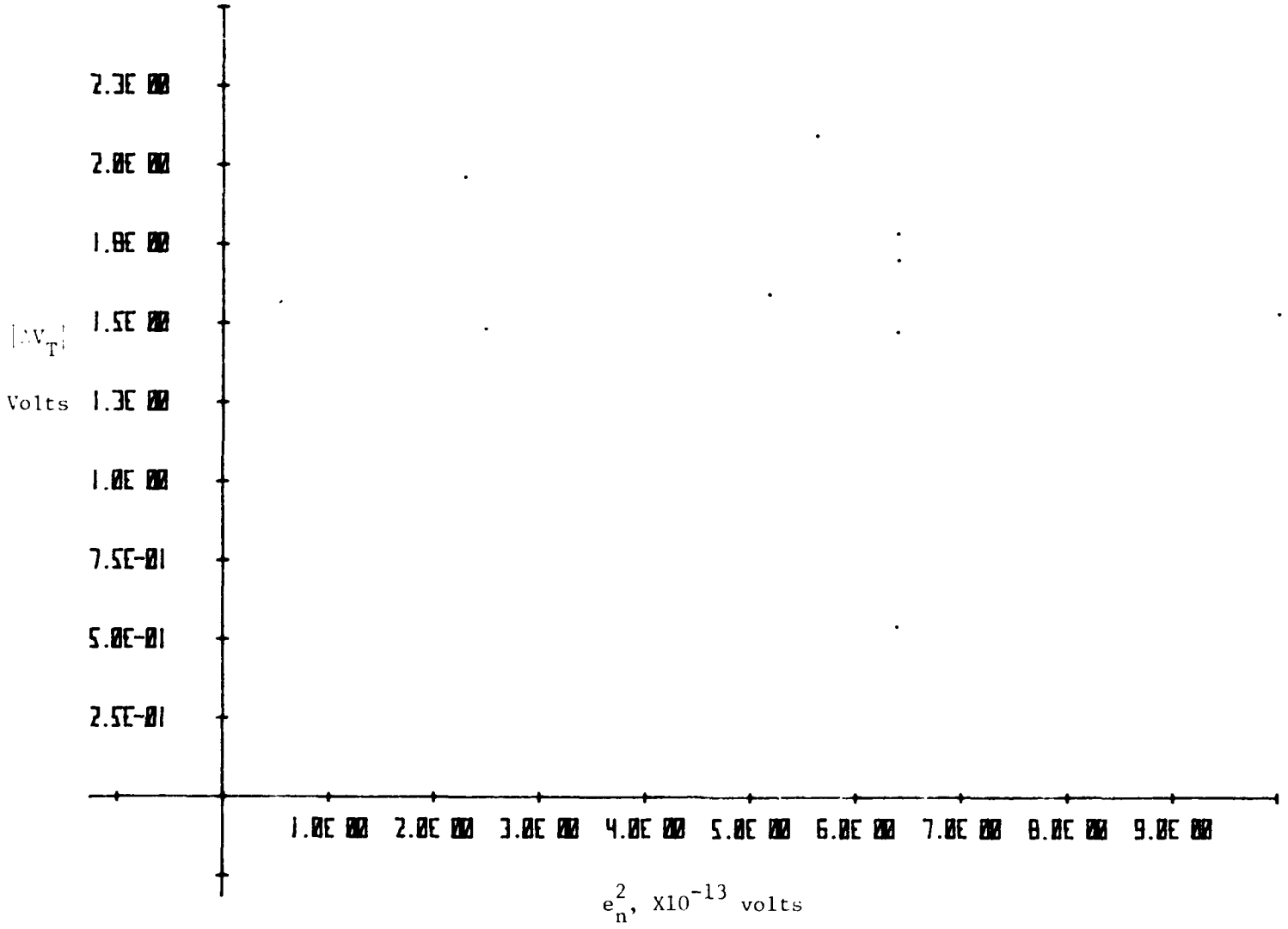


Figure 12. Threshold Voltage Shift as a Function of Equivalent Gate Voltage. R = -0.22 ± 0.34

sources. The necessity of biasing the transistors on produces an additional noise source as indicated by Aoki, Katto, and Yamada (ref. 14). Aoki et al., have found that conductance mobility fluctuations due to surface potential roughness contribute to noise. However, Aoki concludes that "measurements of 1/f noise at low current levels will provide an effective means of monitoring various processes." Pepper (ref. 15) concludes that "the potential fluctuations due to the pairs are weak and consequently they do not show up in conventional C-V or G-V techniques." Pepper's remarks suggest that it may be impossible to detect hole trap dipoles using a room temperature measurement.

Because of the rapid falloff of the electric field produced by dipoles, only those dipoles very near the interface can be expected to produce surface states. Hole traps deep in the oxide may go undetected.

10. CONCLUSIONS

For edge state determinations to be useful as a screen, it first must be established that the shallow surface states produced by hole trap dipoles can be detected at room temperature. If these states can be detected, then noise measurements will be useful if (1) the noise in strong inversion is dominated by these charges and (2) the dipole density at the interface is an indicator of the oxide hardness.

To conclusively verify the value of noise measurements, hard and soft oxides should be evaluated and all radiation tests conducted at low levels.

SECTION VI
DETECTION OF DIPOLE CHARGE

1. OBJECTIVE

The objective of this experiment was to correlate the relative magnitude of total oxide charge measured by noise techniques to the radiation susceptibility of test devices. It was hypothesized that the total oxide charge may include dipole charge associated with hole traps.

2. RATIONALE

Pepper (ref. 15) has given evidence that the hole trap consists of a dipole charge in the oxide. Nicollian and Melchior (ref. 16) have shown that oxide charges alter the surface potential in local regions. The distribution of surface potential affects the spectrum of noise in a manner which allows calculation of σ, the standard deviation of surface potential. σ, in turn is related to Q, the total oxide charge. If the oxide total charge includes Pepper's dipoles, then determination of σ should act as a hardness assurance screen.

3. PROCEDURE

To obtain σ, the log of the squared noise voltage is plotted against the log of frequency. An asymptote of slope 0 is fit to the low frequency data, which should approach a zero slope. Another asymptote of slope 1/f is fit to the higher frequency data and is tangent to the data at the point F_p. The intersection of the two asymptotes occurs at the point F_L. Taking the frequency values of F_p and F_L, σ can be approximated from:

$$F_L = F_p \exp\left[-(\pi 2)^{1/2}\sigma\right] \qquad \text{(Eq. 12)}$$

4. SAMPLES

Ten RCA 40468A MOSFETs were evaluated using noise measurements. The 40468A is an N-channel depletion mode DMOS device with no gate protection.

5. ELECTRICAL TESTS

The HP4470A Transistor Noise Analyzer was used to obtain the noise spectrum data. Drain voltage and drain current were picked to maximize the bandwidth over which measurements could be made.

6. RESULTS

Unfortunately, the bandwidth of the HP4470A Transistor Noise Analyzer was not sufficient to accurately determine F_L and F_p as indicated by Figure 13. No line segment with slope of either 0 of 1/f can be resolved within the band of frequencies accessible. Therefore, determination of σ from the HP4470A measurements does not appear feasible.

7. IMPROVEMENTS

R. Maier* has suggested that σ can also be obtained from the spread of the conductance versus frequency curve for MOS capacitors. Preliminary work is being done in this area, but no results are available for presentation.

Another possible area of investigation is based on the work of Aoki, Kato and Yamada (ref. 14). Aoki et al. noted that the noise of "on" MOSFETs increased as drain current was decreased. This effect was attributed to an increase in surface potential roughness at low electron concentrations, where the charge screening effects of electrons become

*Private Communication with Roe Maier of AFWL.

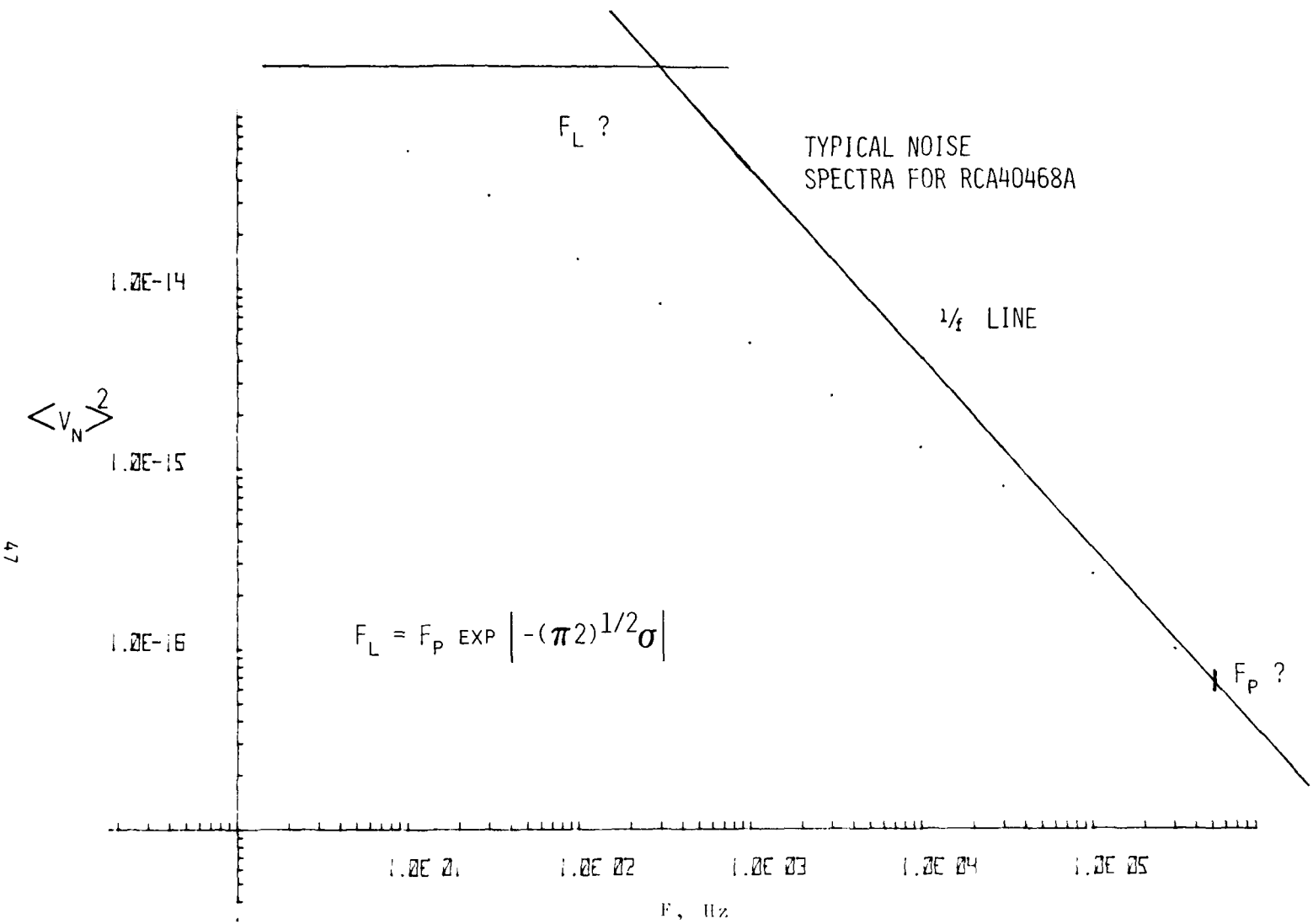


Figure 13. Typical Noise Spectra For RCA 40468A
I_D = 100 μA V_D = 5 V

important. This explanation is remarkably similar to Fowler's (ref. 17) explanation of the low temperature substrate bias effect which Pepper related to hardness. Fowler concludes that "the fluctuations are much more effectively screened than expected as the electrons are forced to the surface." The increase in noise at low drain currents may be a room temperature substitute for the low temperature substrate bias effect. Such measurements would be perfectly suited for the 4470A.

8. CONCLUSION

In conclusion, the HP4470A is not capable of producing data for the evaluation of the standard deviation of surface potential as a total dose screen. However, other methods of analyzing oxide charge show promise and should be explored.

SECTION VII
INPUT CURRENT OF INTEGRATED AMPLIFIERS

1. OBJECTIVE

The objective of this experiment was to provide additional support to the observation that input bias current is related to the hardness of linear amplifiers.

2. RATIONALE

The change in offset voltage is the most important total dose effect in linear bipolar amplifiers. Because of the gain in successive circuit stages, it is reasonalbe to assume that the change in offset voltage in the first stage will dominate the overall response. Therefore, the relative emitter current levels in the input transistors should be a indicator of how much offset voltage change will occur in the amplifier.

3. JUSTIFICATION

The input transistor operating current is the basis for a screen which has been implemented by JPL (ref. 18) and NRL (ref. 19) on LM108 operational amplifiers. The original idea of input current as a screen was developed by Johnston and Skavland (ref. 20), who used input current as a neutron effects screen.

4. PROCEDURE

The offset voltage of test samples was determined along with the necessary information to determine emitter current. The devices were then irradiated and the offset voltage remeasured. The change in offset voltage was then correlated with the average emitter current of the input stage.

5. SAMPLES

Twenty-five Fairchild μA741HC operational amplifiers and 25 TI μA733CN video amplifiers were obtained as test samples. The equivalent circuit of the 741 is shown in Figure 14 and the equivalent circuit of the 733 is shown in Figure 15.

6. ELECTRICAL TESTS

Offset voltage of the samples was measured using a Tektronix 577 curve tracer with a Tektronix 178 Linear IC Test Fixture. A difference amplifier was required at the outputs of the 733 to enable the offset voltage measurement to be made. Care was taken to ensure that the difference amplifier did not contribute to the offset voltage measured. The gain select nodes of the 733 were biased to yield a gain of 100. Plus and minus supply voltages of the 741 were 15V. Supply voltages of the 733 were plus and minus 6 volts.

To obtain input operating current, the output voltage of the op amp was adjusted to 0 volts and the voltage at the offset null nodes recorded. The amplifier was then removed from the test fixture and the impedance between the offset null and V- was recorded, with the positive lead of the ohmmeter connected to the offset null pin. The current through R_1 and R_2 of Figure 14 can be calculated as the offset null voltage divided by the measured value of R_1 or R_2, depending on which side was tested. From circuit analysis theory, it can be seen that the current through R_1 and R_2 is approximately equal to the emitter current of Q_1 and Q_2, respectively. The average emitter current is then calculated as the input operating current.

Similar techniques were used to calculate the input operating current of the 733. Measurements were made between G_1 and G_2 as shown in Figure 15.

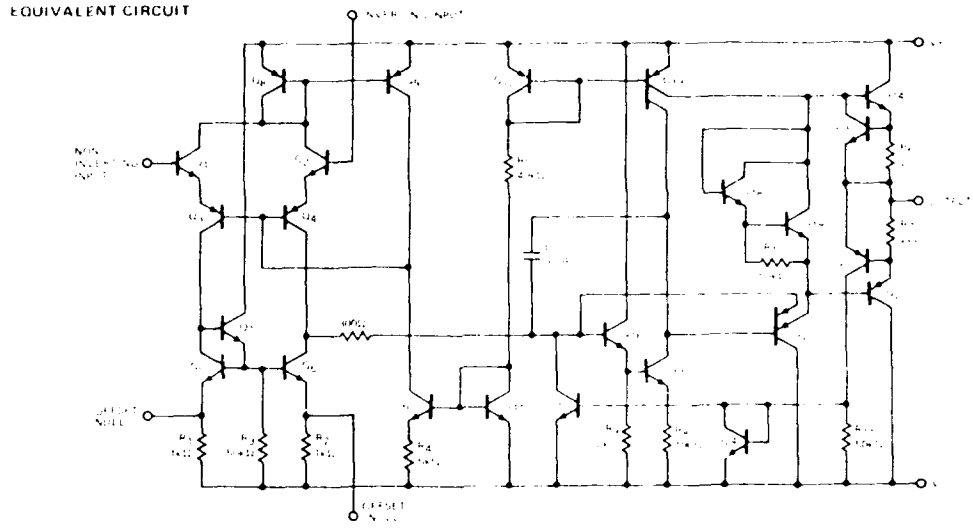


Figure 14. Equivalent Circuit of the 741 Operational Amplifier

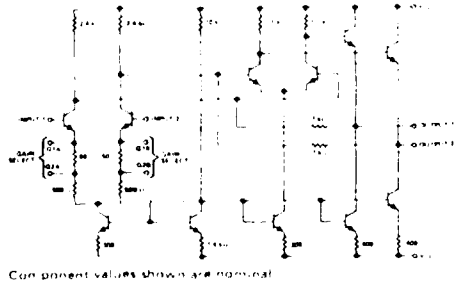


Figure 15. Equivalent Circuit of the 733 Video Amplifier

7. RESULTS

The average input operating current for the 25 741's was 6.85 nA with a standard deviation of 9.82. The average input operating current for the 733's were 1.85 mA with a standard deviation of 0.029. Because the standard deviation of the input operating current is small compared to the expected deviation in offset voltage changes, the 733's were dropped from the experiment.

8. IRRADIATION

The test devices remaining were irradiated by exposure to the AFWL 5 kilocurie Co^{60} gamma ray source. The devices were irradiated to a total ionizing dose of 1×10^{6} Rad (Si). During the irradiation, the devices were configured as unity gain amplifiers as shown in Figure 16.

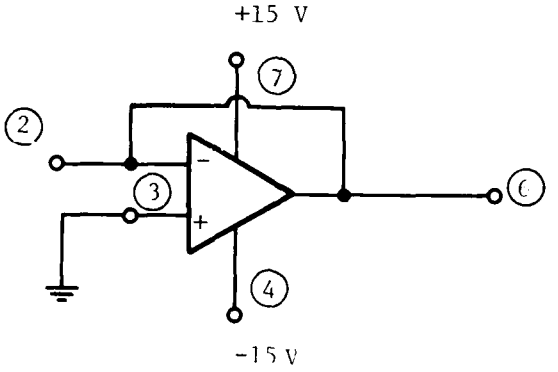


Figure 16. Irradiation Bias Configuration

9. RESULTS

A plot of the change in offset voltage as a function of the input operating current is shown in Figure 17. A least squares fit to the data is also shown.

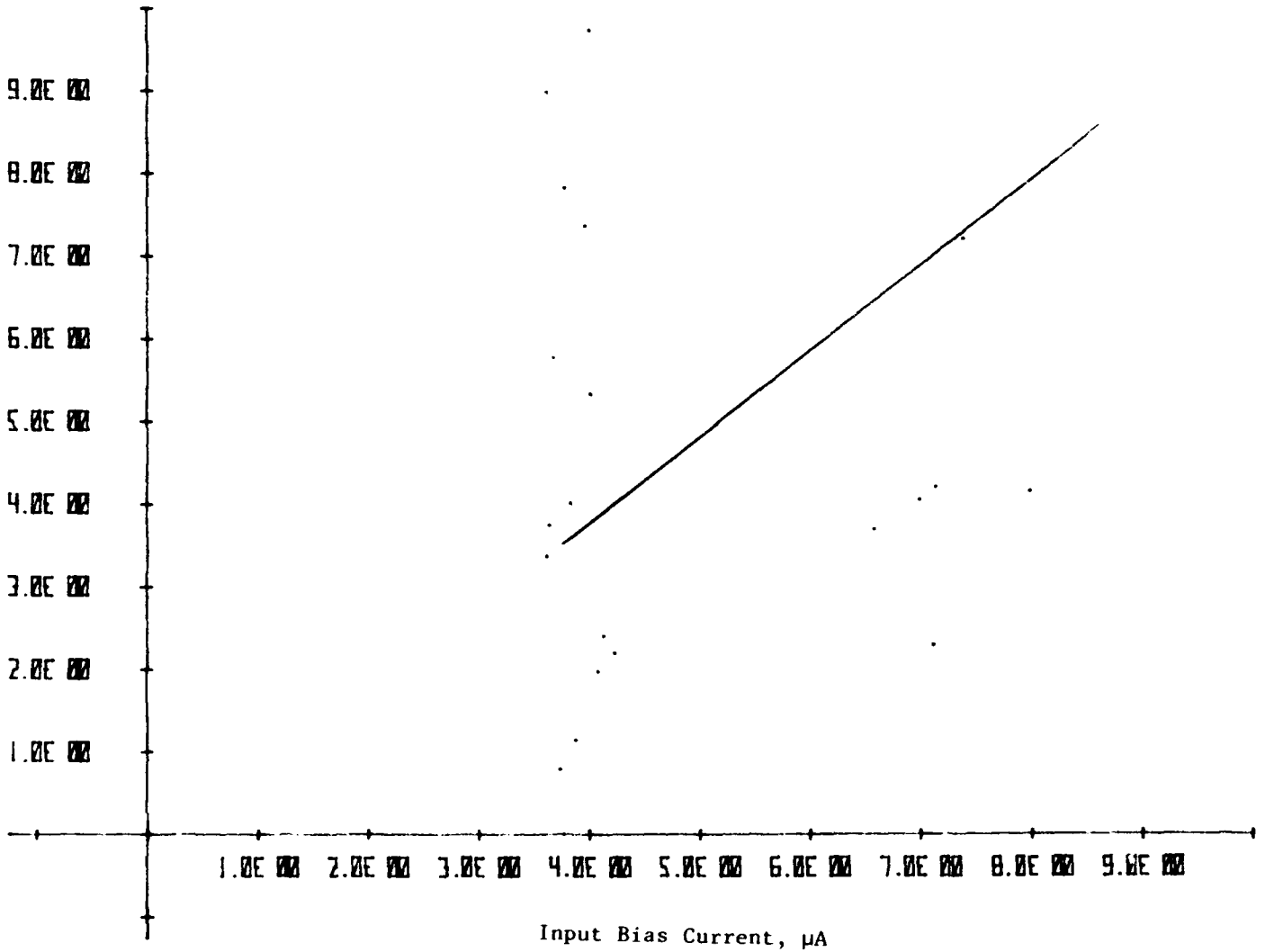


Figure 17. Change in Offset Voltage as a Function of the Average Input Bias Current. R = 0.59 ± 0.14

The positive slope of the fitted line and the poor correlation coefficient indicate that input operating current was not an indicator of total dose hardness for this set of experimental conditions.

10. CONCLUSIONS

The results obtained in this experiment do not conclusively prove or disprove the hypothesis that input bias currents may be used as a screen for operational amplifiers. JPL used input bias current as a diffusion lot screen and not as a discrete parts screen. The data of Figure 17 suggests that test devices were from two diffusion lots. Therefore, only two data points are available to determine if input bias could be a lot screen for 741 operational amplifiers. Two data points are insufficient to determine the validity of the technique as a lot screen. As a part level screen it certainly appears invalid for the mA741. However, the test vehicle chosen for the phase II tests will allow the input operating current to be varied over a wide range such that the spread in $\Delta\ 1/\beta$ of the input transistor can be determined at several different current levels and compared to the spread in average $\Delta\ 1/\beta$ between the current levels. This will indicate how well the technique will work as a function of the maximum spread in input operating current.

SECTION VIII
IRRADIATE AND ANNEAL

1. OBJECTIVE

The objective of this experiment was to verify that annealing reduces total dose damage to an acceptable level and that an equivalent reirradiation exposure will produce a comparable level of damage.

Irradiate and Anneal (IRAN) is a 100 percent screen applicable to any silicon technology device. The devices are exposed to the expected threat level dose under worst case bias conditions and any devices not meeting the threat level are rejected. The remaining devices are annealed and used in the system.

2. JUSTIFICATION

IRAN has been studied by several investigators (refs. 21, 22, 23, 24, and 25). Mixed results have been obtained for the wide range of techniques tried. For IRAN to be implemented as a screen, it must possess two features. First, it must be verified that enough damage can be annealed out to allow the device to pass its electrical specifications and not degrade the failure rate. Secondly, it must be demonstrated that upon reirradiation, the level of damage at the same dose as the original irradiation will produce a comparable amount of damage.

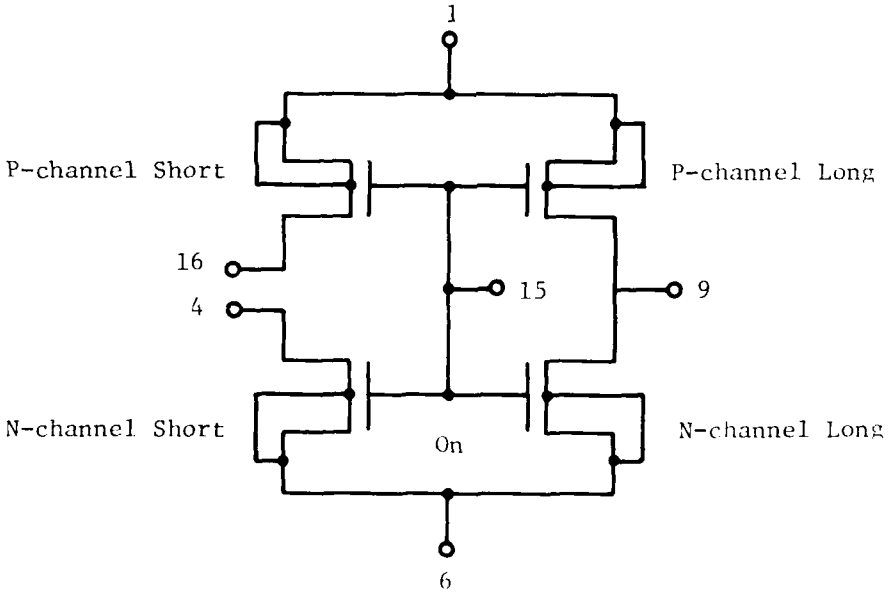
3. PROCEDURE

The test devices in this experiment were split into three groups. The groups were irradiated at 1×10^5, 5×10^5, and 1×10^6 Rad (Si) by Harris Semiconductor. The devices were then annealed. Many annealing times and temperatures have been tried by various investigators with wide results. An anneal bake at 300°C for 6 hours was chosen. The devices were then reirradiated under the same conditions as the first irradiation.

4. SAMPLES

The test samples used were 26 special test structures supplied by Harris Semiconductor. Figure 18 is a circuit diagram of the four MOS transistors. The structure consists of two N-channel and two P-channel devices. One of the N/P channel devices has a short channel while the other has a long channel. The devices were manufactured using hard and soft processes.

Circuit:



Bias for Irradiations: +10 Volts to pins 1 and 15
0 Volts to pin 6
Short pin 4 to pin 16

Figure 18. Harris Semiconductor Special MOSFET Test Structure

5. ELECTRICAL TESTS

The threshold voltage of each device on every unit was determined by measuring the gate voltage at which the drain current equaled 1μA. The drain voltage was set equal to the gate voltage. Harris Semiconductor made the threshold voltage measurements before and after the first irradiation.

6. IRRADIATION

The first irradiations were conducted by Harris Semiconductor. The second irradiations were conducted by BDM using the AFWL 5 kilocurie Co^{60} source. Three separate irradiations were conducted to duplicate the original levels of 1×10^5, 5×10^5, and 1×10^6 Rad (Si). The bias used for all irradiations is given in Figure 18.

7. RESULTS

The statistical results of the experiment are listed in Table 7. The change in threshold voltage produced by the initial irradiation is plotted as a function of the change in threshold voltage produced by the second irradiation in **Figures 19a-d. The correlation coefficient** and least squares fit line is included on each plot.

The information in Table 7 indicates that a sputter metallization process produces damage very similar to the damage caused by total ionizing dose. Referring to Figure 10, if sputtering produces a damage equivalent to dose X_2, then any additional irradiation will cause a negative change in the threshold voltage shift. A negative threshold voltage shift is observed for the sputter metallized devices.

The sputter damage phenomenon also explains why the anneal bake was much more successful for the flash metallized parts. The anneal bake removed part of the sputter produced damage.

TABLE 7. IRAN RESULTS

	ΔV_T								V_T(Initial)/V_T(Anneal)							
	Flash				Sputter				Flash				Sputter			
	N-Channel		P-Channel		N-Channel		P-Channel		N-Channel		P-Channel		N-Channel		P-Channel	
	Short	Long	Short	Long	Short	Long	Short	Long	Short	Long	Short	Long	Short	Long	Short	Long
N	19	11	25	15	11	6	11	6	25	24	25	24	11	11	11	11
$\bar{X}$	0.60	0.65	-0.28	-0.32	-0.97	-1.91	-2.23	-2.96	0.91	0.92	0.97	0.97	0.76	0.76	1.14	1.15
σ	0.32	0.34	0.12	0.14	1.16	1.33	1.16	1.28	0.039	0.041	0.023	0.023	0.083	0.082	0.039	0.037
Max	1.25	1.25	-0.15	-0.15	0.50	0.45	-0.70	-0.80	0.97	1.01	1.01	1.00	0.87	0.87	1.23	1.22
Min	0.20	0.25	-0.55	-0.60	-2.50	-2.95	-3.75	-3.95	0.82	0.082	0.93	0.93	0.65	0.67	1.10	1.10

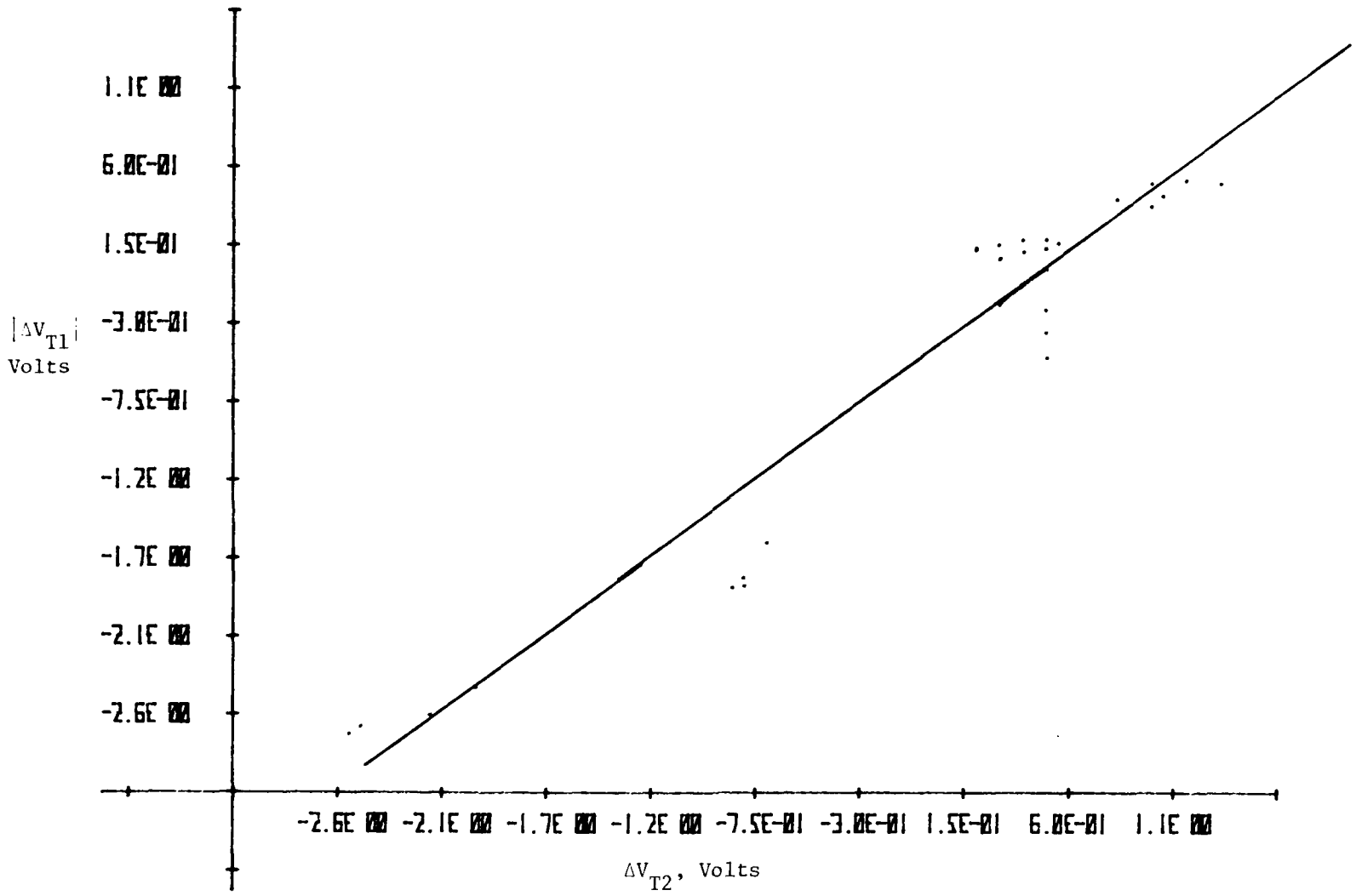


Figure 19a. Comparison of Damage Produced Between First and Second Irradiation. Short N-Channel Devices. R = 0.96

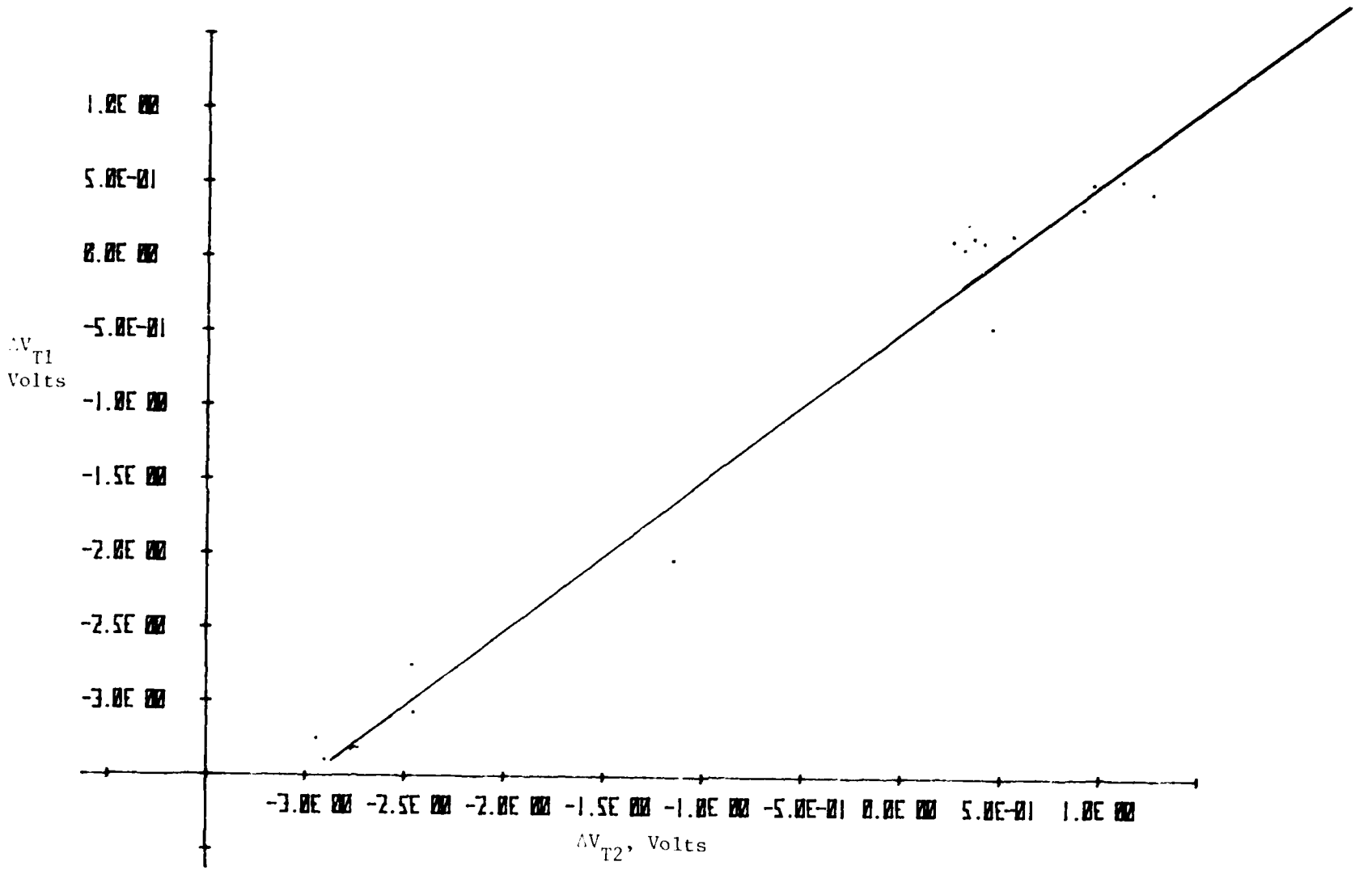


Figure 19b. Comparison of Damage Produced Between First and Second Irradiation. Long N-Channel Devices. R = 0.987

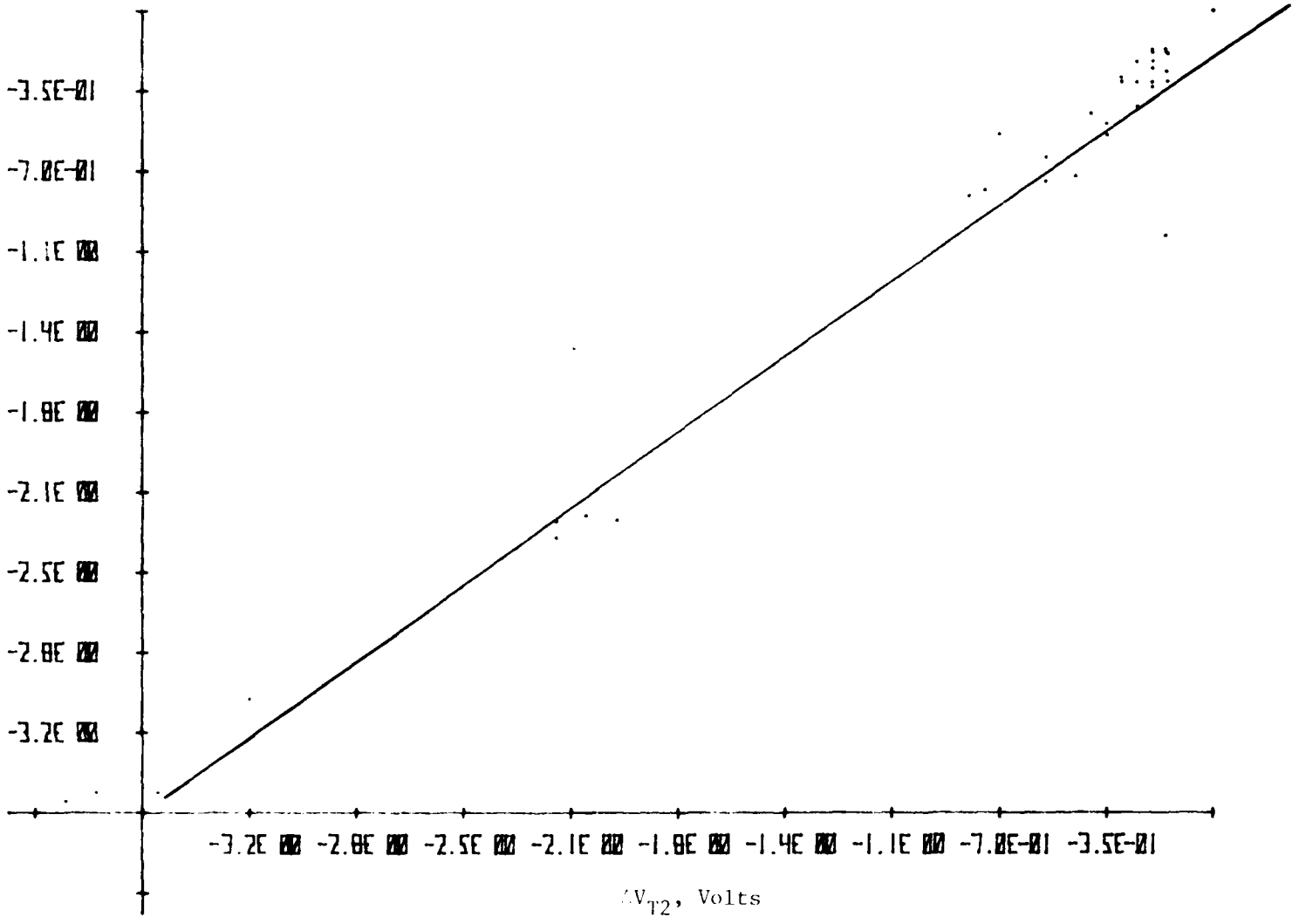


Figure 19c. Comparison of Damage Produced Between First and Second Irradiation. Short P-Channel Devices. R = 0.987

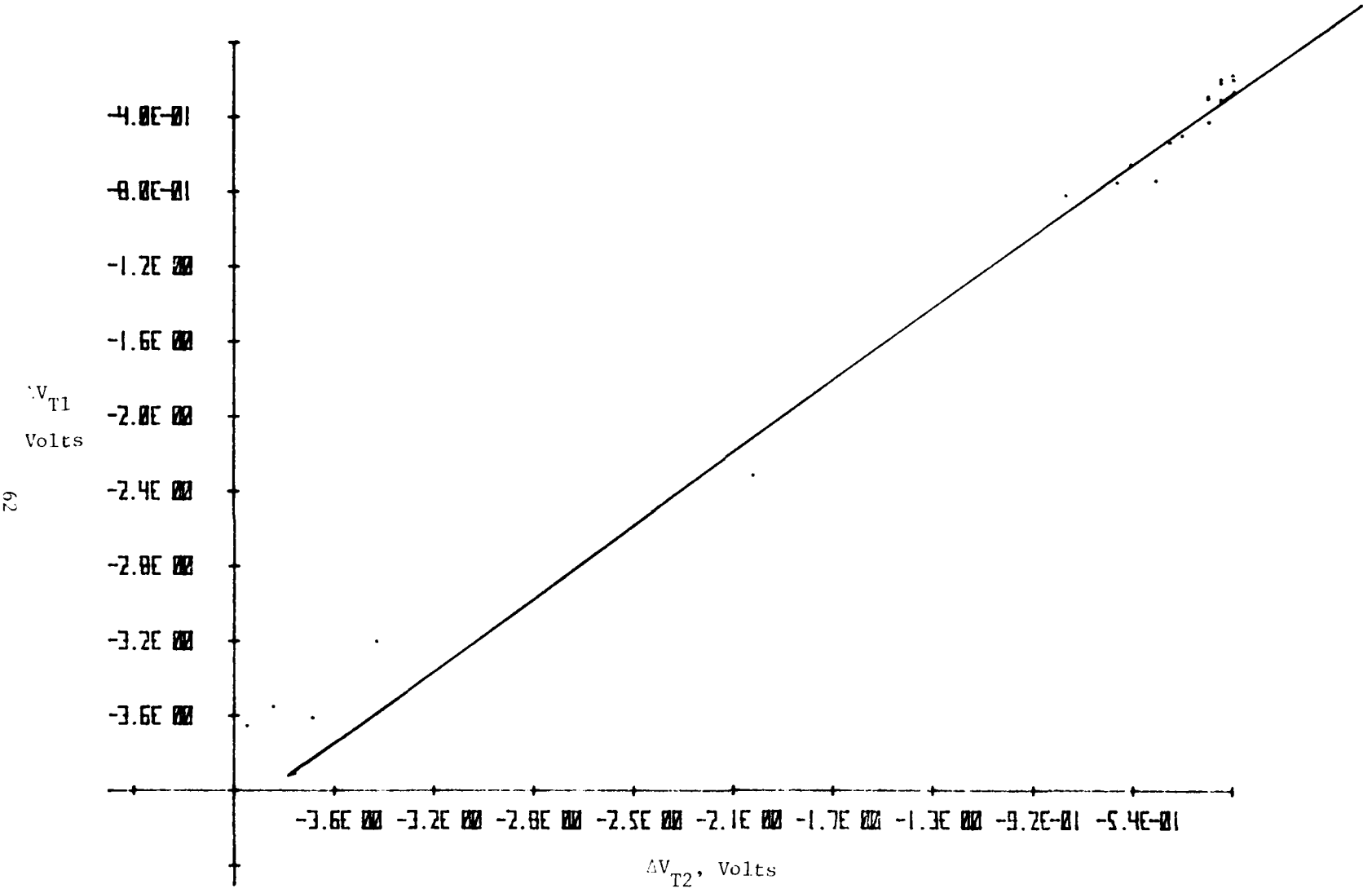


Figure 19d. Comparison of Damage Produced Between First and Second Irradiation. Long P-Channel Devices. R = 0.996

The results of Table 7 indicate that annealing is much more successful on P-channel devices than on N-channel structures. The reason for this effect is not clear.

The results of Figures 19a-d show a good correlation between the threshold voltage shift produced by the first and second irradiation. The correlation suggests that radiation damage is reproducible after an anneal bake.

A disturbing feature of Figures 19a-d is the good fit shown by the sputtered devices. If the anneal had been completely successful, the sputtered parts should have shown the positive threshold voltage shift experienced by the flash metallized parts. An explanation for this effect has not yet been developed.

8. CONCLUSION

The overall results obtained in this IRAN experiment support the use of IRAN as a total dose screen, if the annealing is performed at a sufficiently high temperature.

SECTION IX
SUMMARY AND CONCLUSIONS

A summary of the results obtained in the phase I verification testing is given in Table 8. The technique is listed along with the parameters which were correlated and the results of the correlation. The test vehicle and sample size are also given.

The most positive results obtained were for the IRAN tests on the discrete MOS devices. Although these preliminary verification tests (except for IRAN) were inconclusive, they provided much insight for future tests. It is now believed that E-B avalanche tests should be performed on gated devices in order to control hole injection into the oxide. It became obvious that in order for the input operating current to be sensitive to the radiation induced shift in offset voltage, there must be a large variation in the operating current from device to device or lot to lot.

An approach other than the one selected in these tests will have to be taken in order to measure the room temperature effects of dipoles at the interface. BDM is currently investigating the use of conductance versus frequency curves.

The results that were particularly disappointing were those for the hole injection techniques. It was hoped that various "stress" tests could be used to simulate the effects of ionizing radiation by causing hole trapping and interface state generation. Part of the problem with the results obtained may have been due to the test vehicle chosen. It was discovered, after the tests had been performed, that the 40468A is a DMOS device. Although this should not invalidate the results, the structure presents additional variations from a conventional MOSFET which could make the data interpretation more difficult.

In addition to the nonconventional structure used for the stress tests, the approach taken was too simplistic. It is well known that damage as a function of dose is nonlinear and saturates at some level. The "growth curves" for stress have not been characterized but they

TABLE 8. SUMMARY OF PHASE I VERIFICATION TEST RESULTS

	TECHNIQUE	TEST VEHICLE	SAMPLE SIZE	PARAMETERS CORRELATED	CORRELATION COEFFICIENT
1.	Avalanche hole injection	RCA 40468A	10	$\Delta V_G(\text{stress}) : \Delta V_T(\gamma)$ [for constant BV]	-0.355 ± 0.31
2.	Negative bias temperature stress	40468A MOSFET	7	$\Delta V_T(\text{stress}) : \Delta V_T(\gamma)$	0.83 ± 0.14
			15	$\Delta V_T(\text{stress}) : \Delta V_T(\gamma)$	-0.304 ± 0.25
				$\Delta\mu(\text{stress}) : \Delta\mu(\gamma)$	-0.121 ± 0.27
3.	E-B avalanche on bipolar transistors	2N3468 PNP, power	10	$\Delta 1/\beta(\text{stress}) : \Delta 1/\beta(\gamma)$	-0.11 ± 0.35
		2N2720 NPN, low power	10	$\Delta 1/\beta(\text{stress}) : \Delta 1/\beta(\gamma)$	0.64 ± 0.21
		2N2944 PNP, low power	10	$\Delta 1/\beta(\text{stress}) : \Delta 1/\beta(\gamma)$	0.62 ± 0.22
		2N2537 NPN, switch	10	$\Delta 1/\beta(\text{stress}) : \Delta 1/\beta(\gamma)$	-0.64 ± 0.21
4.	Edge states by low frequency noise	40468A MOSFET	10	e_n^2 (10Hz) : $\Delta V_T(\gamma)$	-0.22 ± 0.34
5.	Dipole density from noise versus frequency	40468A MOSFET		No results (could not measure γ from e_n^2 versus frequency)	
6.	Input operating of linear circuits	µA741 op amp.	25	$I_1 : \Delta V_{off}(\gamma)$	0.59 ± 0.14
		µA733 video amp.	25	No results (spread in I_1 too small)	
7.	IRAN	Special P and N-Channel test Transistors from Harris Semiconductor		N-Channel $\Delta V_T(\gamma_1) : \Delta V_T(\gamma_2)$ short	0.960
				N-Channel $\Delta V_T(\gamma_1) : \Delta V_T(\gamma_2)$ long	0.987
				P-Channel $\Delta V_T(\gamma_1) : \Delta V_T(\gamma_2)$ short	0.987
				P-Channel $\Delta V_T(\gamma_1) : \Delta V_T(\gamma_2)$	0.996

are assumed also to be nonlinear. A more thorough approach to the verification of the stress test technique would involve a complete characterization of the parameter shift versus stress curve at several different electric field strengths. These could then be compared to the ΔV_T versus dose curves in order to identify similarities in slope and to best select an appropriate stress and dose level to determine correlation.

In conclusion, the phase I verification tests have provided valuable information on how to conduct the phase II verification tests, even though these preliminary results were not encouraging.

REFERENCES

1. Verwey, J. F., "Avalanche Injected Hole Currents in SiO_2," App. Phys. Lett., Vol. 21, No. 9, November 1972.

2. Verwey, J. F., "Hole Currents in Thermally Grown SiO_2," J. Appl. Phys., Vol. 43, No. 5, May 1972.

3. Bakowski, M., R. H. Cockrum, N. Zamani, J. Maserjian and C. R. Viswanathan, "Trapping Effects in Irradiated and Avalanche-Injected MOS Capacitors," IEEE-Trans. on Nucl. Sci., Vol. NS-25, No. 6, December 1978.

4. Freeman, R. and A. Holmes-Siedle, "A Simple Model for Predicting Radiation Effects in MOS Devices," IEEE Trans. on Nucl. Sci., Vol. NS-25, No. 6, December 1978.

5. Deal, B. E., M. Sklar, A. S. Grove and E. H. Snow, "Characteristics of the Surface Change (Qss) of Thermally Oxidized Silicon," J. Electrochem. Soc., Vol. 114, No. 3, p. 266, 1967.

6. Goetzberger, A., A. D. Lopez and R. J. Strains, J. Electrochem Soc., Vol. 120, No. 90, 1973.

7. Jeppson, K. O. and C. M. Svensson, J. Appl. Phys., Vol. 48, No. 5, May 1977.

8. Collins, D. R., IEEE Trans. on Electron Devices, Vol. ED-16, No. 4, April 1969.

9. McDonald, B. A., IEEE Trans. on Electron Devices, Vol. ED-17, No. 10, October 1970.

10. Verwey, J. F., Solid State Elec., 14, 775, 1971.

11. Pepper, M., "The Radiation Hardness of the Si-SiO_2 Interface and Carrier Localization in The Inversion Layer," J. Phys. and Chem. Solid State, Vol. 10, 1977.

12. Pepper, M., The Physics of SiO_2 and its Interfaces, New York: Pergamon Press, 1978, p. 407.

13. Sah, C. T. and F. H. Hielscher, "Evidence of The Surface Origin of the 1/f Noise," Phys. Rev. Lett., Vol. 17, No. 18, October 1966.

REFERENCES (Concluded)

14. Aoki, M., H. Katto, and E. Yamada, "Low Frequency 1/f Noise in MOSFETs at Low Current Levels," J. Appl. Phys., Vol. 48, No. 12, December 1977.

15. Pepper, M., "Inversion Layer Transport and the Radiation Hardness of the Si-SiO_2 Interface," IEEE Trans. on Nucl. Sci., Vol. NS-25, No. 6, December 1978.

16. Nicollian, E. and H. Melchior, "A Quantitative Theory of 1/f Type Noise Due to Interface States in Thermally Oxidized Silicon," The Bell System Technical Journal, November 1967.

17. Fowler, A. B., "Substrate Bias Effects on Electron Mobility in Silicon Inversion Layers at Low Temperatures," Phys. Rev. Lett., Vol. 34, No. 1, January 1975.

18. Gauthier, M. K. and A. G. Stanley, Jet Propulsion Laboratory Report 900-856, prepared for DNA, December 1977.

19. Palkuti, L., private communications.

20. Johnston, A. H. and R. L. Skavland, "Terminal Measurements for Hardness Assurance in TTL Devices," IEEE Trans. on Nucl. Sci., Vol. NS-22, No. 6, December 1975.

21. Arimura, I., et al., "A Study of Electronics Radiation Hardness Assurance Techniques," AFWL-TR-73-134, January 1974.

22. Poch, W. and A. G. Holmes-Siedle, "A Prediction and Selection System for Radiation Effects in Planar Transistors," IEEE Trans. on Nucl. Sci., Vol. NS-15, No. 6, December 1968.

23. Stanley, A. G. and W. E. Price, IEEE Trans. on Nucl. Sci., Vol. NS-23, No. 6, December 1976.

24. Nelson, D. L. and R. J. Sweet, IEEE Trans. on Nucl. Sci., Vol. NS-13, No. 6, December 1966.

25. Stanley, A. G., K. E. Martin and W. E. Price, Jet Propulsion Laboratory Pub. 77-41, Vol. 1.

BIBLIOGRAPHY

The following bibliograpy is a list of the articles obtained and reviewed for this program listed in alphabetical order by author. Two additional sources were not included in this bibliography because of the shear volume of relevant articles. Several hundred articles pertinent to semiconductor total dose reponse, hardening, and hardness assurance, are published in the IEEE Transactions on Nuclear Science No. 6 published each December. This issue contains selected papers presented at the annual IEEE Conference on Nuclear and Space Radiation Effects. This conference was started in 1964 with conference papers being published in the November issue for 1964 and the October issue in 1965. From 1966 the conference papers have appeared in the December issue. A recent publication which contains numerous articles of interest for total dose phenomena in semiconductors is the Proceedings of the International Topical Conference on the Physics of SiO_2 and Its Interfaces. The papers presented at this conference have been published in book form by Pergamon Press titled The Physics of SiO_2 and Its Interfaces, editor Sokrates T. Pantelides, 1978, Pergamon Press., Inc.

BIBLIOGRAPHY

1. Adler, M. S. "A New Noncapacitive Method of Determining Net Surface Charge Densities Using Floating Field Ring Devices," IEEE Trans. on Electron Devices, ED-25 No. 9, September 1978.

2. Anderson, P. W. "The Fermi Glass: Theory and Experiment," Concepts on Solid State Physics, Vol. 2, 1970.

3. Anderson, P. W. "Absence of Diffusion in Certain Random Lattices," Physical Review, Vol. 109, No. 5, March 1958.

4. Aoki, M., H. Katto and E. Yamada. "Low-Frequency 1/f Noise in MOSFET's at Low Current Levels," J. Appl. Phys., 48(12), December 1977.

5. Arimura, I. et al. "A Study of Electronics Radiation Hardness Assurance Techniques," AFWL-TR-73-134, 3 Volumes, January 1974.

6. Arnold, E. "Surface Charges and Surface Potential in Silicon Surface Inversion Layers," IEEE Trans. on Elect. Devices, Vol ED-15 No. 12, December 1968.

7. Aubuchon, K. G., E. Harari, and P. Chang. "CMOS Radiation Hardening," Hughes report HAC-P75-116, October 1974.

8. Ausman, G. A. and F. B. McLean. "Electron-Hole Pair Creation Energy in SiO_2," Appl. Phys. Letters, Vol. 26, No. 4, 15 February 1975.

9. Beckmann, K. H. and N. J. Harrick. "Hydrides and Hydroxyls in Thin Silicon Dioxides Films," J. Electrochem. Soc., Vol. 118, No. 4, April 1971.

10. Bennett, A. J. and L. M. Roth. "Electronic Structure of Defect Centers in SiO_2," J. Phys. Chem. Solids, Vol. 32, pp. 1251-1261, 1971.

11. Berglund, C. N. "Surface States of Steam-Grown Silicon-Silicon Dioxide Interfaces," IEEE Trans. on Elect. Devices, Vol. ED-13, No. 10, October 1966.

12. Berglund, C. N. and R. J. Powell. "Photoinjection into SiO_2: Electron Scattering in the Image Force Potential Well," J. Appl. Phys., Vol. 42 No. 2, February 1971.

13. Blanc, J. "A Revised Model for the Oxidation of Si by Oxygen," Appl. Phys. Letters, Vol. 33 No. 5, 1 September 1978.

14. Breed, D. J. "Non-Ionic Room Temperature Instabilities in MOS Devices," Solid-State Electronics, Vol. 17, pp. 1229-1243, 1974.

15. Brotherton, S. D., T. G. Read, D. R. Lamb, and A. F. W. Willoughby. "Surface Charge and Stress in the Si/SiO_2 System," Solid-State Electronics, Vol. 16, pp. 1367-1375, 1973.

16. Brown, G. A. "Radiation Hardened Test Structures," Texas Instruments Report No. 03-77-10, March 1977.

17. Brugler, J. S. and P. G. A. Jespers. "Charge Pumping in MOS Devices," IEEE Trans. on Elect. Devices, ED-16 No. 3, March 1969.

18. Bruncke, W. C. et al. "Techniques for Screening Bipolar Transistor Degradation Due to Ionizing Radiation," Texas Instruments Report 03-74-33, November 1974, for NAD Crane (Report TR/7024/C74/121).

19. Buehler, M. G. and D. E. Sawyer. "Microelectronic Test Patterns and Production of Custom ICs," Circuits Manufacturing, Vol. 17, No. 2, February 1977.

20. Burghard, R. A. "Process Dependence of MOS Radiation Sensitivity," presented at IEEE workshop, December 7, 1973, Washington, D.C.

21. Buxo, J., D. Esteve, G. Enea, and A. Martinez. "A 'Four-Parameters' Model That Fits the Degradation Curve ΔV_G (V_G) of MOS Transistors Under Irradiation," Solid-State Electronics, Vol. 15, pp. 1029-1031 1972.

22. Cabrera, N. and N. F. Mott. "Theory of the Oxidation of Metals," Report on Progress in Physics, Vol. 12, 1948-49.

23. Castagne, R. and A. Vapaillo. "Description of the SiO_2-Si Interface Properties by Means of Very Low Frequency MOS Capacitance Measurements," Surface Science, Vol. 28, pp. 157-193, 1971.

24. Chang, C. C. and W. C. Johnson. "Distribution of Flat-Band Voltages in Laterally Nonuniform MIS Capacitor and Application to a Test for Nonuniformities," IEEE Trans. on Elect. Devices, ED-25 No. 12, December 1978.

25. Chang, C. C. and W. C. Johnson "Frequency and Temperature Tests for Lateral Nonuniformities in MIS Capacitors," IEEE Trans. on Elect. Devices, ED-24 No. 10, October 1977.

26. Chou, N. J. "Application of Triangular Voltage Sweep Method to Mobile Charge Studies in MOS Structures," J. Electrochem Soc., Vol. 118, No. 4, April 1971.

27. Chow, T. S. "Theory of Unsymmetric Laminated Plates," J. Appl. Phys., Vol. 46, No. 1, January 1975.

28. Chow, T. S. "Thermal Warping of Layered Composites," J. Appl. Phys., Vol. 47, No. 4, April 1976.

29. Churchill, J. N., T. W. Collins and F. E. Holmstrom. "Electron Irradiation Effects in MOS Systems," IEEE Trans. on Electron. Devices, Vol. ED-21, No. 12, December 1974.

30. Cohen, S. "Total Dose Radiation-Hardened COS/MOS Integrated Circuits," RCA Report PRRL-75-CR-16, March 1975.

31. Collins, D. R. "h_{FE} Degradation Due to Reverse Bias Emitter-Base Junction Stress," IEEE Trans. on Elect. Devices, ED-16 No. 4, 1969.

32. Crabbe, J. S. "Application of MOS Hardening Techniques to Bipolar Device Processing," Texas Instruments Report 03-75-34 for NWSC Crane (Report TR/7024/C74/285), July 1975.

33. Curtis, O. L. Jr. and J. R. Srour. "The Multiple-Trapping Model and Hole Transport in SiO_2," Appl. Phys., Vol. 48, No. 9, September 1977.

34. Curtis, O. L. Jr., J. R. Srour, and K. Y. Chiu. "Hole and Electron. Transport in SiO_2 Films," J. Appl. Phys., Vol. 45, No. 10, October 1974.

35. Danchenko, V., V. D. Desai and S. S. Brashears. "Characteristics of Thermal Annealing of Radiation Damage in MOSFETs," J. Appl. Phys., Vol. 39, No. 5, April 1968.

36. Deal, B. E. "The Current Understanding of Charges in the Thermally Oxidized Silicon Structure," J. Electrochem. Soc., Vol. 121, No. 6, June 1974.

37. Deal, B. E., M. Sklar, A. S. Grove, and E. H. Snow. "Characteristics of the Surface-State Charge (Q_{ss}) of Thermally Oxidized Silicon," J. Electrochem. Soc., Vol. 114, No. 3, March 1967.

38. Deppe, H. R., B. Hasler and J. Hopfner. "Investigations on the Damage Caused by Ion Etching of SiO_2 Layers at Low Energy and High Dose," Solid State Electronics, Vol. 20, pp. 51-55, 1977.

39. Derbenwick, G. F., J. G. Fossum, B. L. Gregory, and H. H. Sander. "Radiation-Hardening of CMOS Integrated Circuits," Sandia Laboratories Report, SAND76-0355, October 1976 (limited distribution).

40. DiMaria, D. J. "Room-Temperature Conductivity and Location of Mobile Sodium Ions in the Thermal Silicon Dioxide Layer of a Metal-Silicon Dioxide-Silicon Structure," J. Appl. Phys., Vol. 48, No. 12, December 1977.

41. DiMaria, D. J., F. A. Weinberg and J. M. Aitken. "Location of Positive Charges in SiO_2 Films on Si Generated by vuv Photons, X-Rays, and High Field Stressing," J. Appl. Phys., Vol. 48, No. 3, March 1977.

42. DiStefano, T. H. "Barrier Inhomogeneities on an Si-SiO_2 Interface by Scanning Internal Photoemission," Appl. Phys. Letters, Vol. 19, No. 8, 15 October 1971.

43. DiStefano, T. H., and D. E. Eastman. "Photoemission Measurements of the Valence Levels of Amorphous SiO_2," Physical Review Letters, Vol. 27, No. 23, 6 December 1971.

44. EerNisse, E. P. "Viscous Flow of Thermal SiO_2," Appl. Phys. Letters, Vol. 30, No. 6, 15 March 1977.

45. Everhart, T. E. and P. H. Hoff. "Determination of Kilovolt Electron Energy Dissipation versus Penetration Distance in Solid Materials," J. Appl. Phys., Vol. 42, No. 13, December 1977.

46. Fahrner, W. R. and Schneider, C. P. "A New Fast Technique for Large-Scale Measurements of Generation Lifetime in Semiconductors," J. Electrochem. Soc., Vol. 123, No. 1, January 1976.

47. Fang, F. F. and A. B. Fowler. "Transport Properties of Electrons in Inverted Silicon Surfaces," Physical Review, Vol. 169, No. 3, May 1968.

48. Fowkes, F. M., W. E. Dahlke and S. R. Butler. "Radiation Effects in MOS Gate Insulators," Harry Diamond Laboratories Report HDL-CR-75-105-1, September 1975.

49. Fowler, A. B. "Substrate Bias Effects on Electron Mobility in Silicon Inversion Layers at Low Temperatures," Physical Review Letters, Vol. 34, No. 1, January 1975.

50. Fowler, A. B., F. Fang, and F. Hochberg. "Hall Measurements on Silicon Field Effect Transistor Structures," IBM Journal, September 1964.

51. Friedrich, H. "Surface Charges Induced by Mechanical Stresses in the Silicon-Silicon Dioxide Interface," Solid-State Electronics, Vol. 14, pp. 639-641, 1971.

52. Fritzsche, C., A. Goetzberger, A. Axmann, W. Rothemund, and G. Sixt. "Effect of Ion-Implantation into Thermal SiO_2-Films on Sodium Ion Drift," Radiation Effects, Vol. 7, pp. 87-93, 1971.

53. Fu, H. and C. T. Sah. "Theory and Experiments on Surface 1/f Noise," IEEE Trans. on Elect. Devices, ED-19, No. 2, February 19[illegible].

54. Gabilli, E., M. Severi, G. Soncini, and Q. Zini. "Electrical Properties of MOS Capacitors With Oxide Grown in the Presence of HCL," Alta Frequenza, Vol. XLI, No. 11, November 1972.

55. Galloway, K. F. and S. Mayo. "Radiation Dose at the Silicon-Sapphire Interface Due to Electron-Beam Aluminization," J. Appl. Phys., Vol. 49 No. 4, April 1978.

56. Galloway, K. F. and P. Roitman. "Some Aspects of Using a Scanning Electron Microscope for Total Dose Testing," National Bureau of Standards Report NBSIR-77-1235, September 1977.

57. Ganthier, M. K. and A. G. Stanley. "Hardening Techniques for Microelectric Circuitry," Jet Propulsion Labs Report 900-856, December 1977.

58. Goetzberger, A., A. D. Lopez and R. J. Strain. "On the Formation of Surface States During Stress Aging of Thermal Si-SiO_2 Interfaces," J. Electrochem. Soc., Vol. 120, No. 1, January 1973.

59. Goetzberger, A. "Ideal MOS Curves for Silicon," Bell Systems Tech. Journal, September 1966.

60. Goetzberger, A., V. Heine and E. H. Nicollian. "Surface States in Silicon from Charges in the Oxide Coating," Appl. Phys. Letters, Vol. 12, No. 3, February 1968.

61. Goetzberger, A. "Improved Properties of Silicon Dioxide Layers Grown Under Bias," J. Electrochem. Soc., Vol. 113, No. 2, February 1966.

62. Gray, P. V. and D. M. Brown. "Density of SiO_2-Si Interface States," Appl. Phys. Letters, Vol. 8, No. 2, January 1966.

63. Greegor, R. B. and L. L. Sivo. "Effects of Process Variations on Total Dose Sensitivities of Bipolar Oxides," Boeing Aerospace Co. Report D180-20519-1, April 1977.

64. Gross, B., J. Dow and S. V. Nablo. "Charge Buildup in Electron-Irradiated Dielectrics," J. Appl. Phys., Vol. 44, No. 6, June 1973.

65. Grove, A. S., O. Leistiko, and C. T. Sah. "Redistribution of Acceptor and Donor Impurities During Thermal Oxidation of Silicon," J. Appl. Phys., Vol. 35, No. 9, September 1964.

66. Grove, A. S. and E. H. Snow. "A Model for Radiation Damage in Metal-Oxide-Semiconductor Structures," Proc. of IEEE, June 1966.

67. Grove. A. S. and D. J. Fitzgerald. "Surface Effects on p-n Junctions: Characteristics of Surface Space-Charge Regions Under Non-Equilibrium Conditions," Solid-State Electronics, Vol. 9, pp. 783-806, 1966.

68. Gwyn, C. W. "Model for Radiation-Induced Charge Trapping and Annealing in the Oxide Layer of MOS Devices," J. Appl. Phys., Vol. 40, No. 12, November 1969.

69. Gwyn, C. W. "Ionizing Radiation Effects in the Insulator Region of MOS Devices," Sandia Laboratories Report SLA-73-0013, January 1973.

70. Gwyn, C. W. "The Radiation Tolerances of MOS Devices," Sandia Laboratories Report SC-RR-69-639, September 1969.

71. Harari, E., S. Wang and B. S. H. Royce. "Low-Temperature Irradiation Effects in SiO_2-Insulated MIS Devices," J. Appl. Phys., Vol. 46, No. 3, March 1975.

72. Hart, A. R., J. B. Smyth Jr., J. P. Raymond, and V. A. J. VanLint. "Hardness Assurance for Long-Term Ionizing Radiation Effects on Bipolar Structures," Defense Nuclear Agency Report DNA 4574F, March 1978.

73. Hofstein, S. R. "Stabilization of MOS Devices," Solid-State Electronics, Vol. 10, pp 657-670, 1967.

74. Holmberg, G. L., A. B. Kuper and F. D. Miraldi. "Water Contamination in Thermal Oxide on Silicon," J. Electrochem. Soc., Vol. 117, No. 5, May 1970.

75. Hsu, S. T., D. J. Fitzgerald, and A. S. Grove. "Surface-State Related 1/f Noise in p-n Junctions and MOS Transistors," Appl. Phys. Letters, Vol. 12, No. 9, May 1968.

76. Hughes, G. W. "Radiation and Charge Transport in SiO_2," RCA report PRRL-77-CR-5, February 1977.

77. Hughes, G. W. "Radiation Effects on the Electrical Properties of MOS Devices Materials," Harry Diamond Laboratories Report HDL-CR-77-088, February 1978.

78. Hughes, H. L. "A Pre-Irradiation Indicator for Total-Dose Ionizing Radiation-Sensitivity," IEEE Trans. on Nuclear Science, Vol. NS-22, No. 5, October 1975.

79. Hughes, R. C. "Hole Mobility and Transport in Thin SiO_2 Films," Appl. Phys. Letters, Vol. 26, No. 8, 15 April 1975.

80. Jacobs, E. P. and G. Dorda. "Optically Induced Charge Storage in Ion Implanted SiO_2," Solid-State Electronics, Vol. 20, pp. 367-372, 1977.

81. Jacobs, E. P. and G. Dorda. "Charge Storage by Irradiation With UV Light in Non-Biased MNOS Structures," Solid-State Electronics, Vol. 20, pp. 361-365, 1977.

82. Jeppson, K. O. and C. M. Svensson. "Negative Bias Stress of MOS Devices at High Electric Fields and Degradation of MNOS Devices," J. Appl. Phys., Vol. 48, No. 5, May 1977.

83. Johnson, N. M., W. C. Johnson, and M. A. Lampert "Electron Trapping in Aluminum-Implanted Silicon Dioxide Films on Silicon," J. Appl. Phys., Vol. 46, No. 3, March 1975.

84. Jones, C. E. and D. Embree. "Correlations of the 4.77-4.28 eV Luminescence Band in Silicon Dioxide with the Oxygen Vacancy," J. Appl. Phys., Vol. 47, No. 12, December 1976.

85. Jorgenson, P. J. "Effect of an Electric Field on Silicon Oxidation," J. Chem. Phys., Vol. 37, No. 4, August 1962.

86. Jorgenson, P. J. "Electrolysis of SiO_2 on Silicon," J. Chem. Phys., Vol. 49, No. 4, August 1968.

87. Kampf, V. and H. G. Wagemann. "Radiation Damage of Thermally Oxidized MOS Capacitors," IEEE Trans. on Elect. Devices, Vol. ED-23, No. 1, January 1976.

88. Kingston, R. H. and S. F. Newstadter. "Calculation of the Space Charge, Electric Field, and Free Carrier Concentration at the Surface of a Semiconductor," J. Appl. Phys., Vol. 26, No. 6, June 1955.

89. Kopp, R. J., T. A. Williamson, and W. W. Grannemann. "Instrumentation Providing Automated Data for Use in Metal-Insulator-Semiconductor Interface Studies," ISA Trans., Vol. 10, No. 2, 1971.

90. Kreutz, E. W. "Photoemission Studies at RT of X-Irradiated MOS Structures," Phys. Stat. Sol., Vol. 13, pp. 557, 1972.

91. Kreutz, E. W. "Slow Relaxation Phenomena on X-Irradiated Real Germanium Surfaces," Thin Solid Films, Vol. 42, pp. 161-167, 1977.

92. Kuhn, M. "A Quasi-Static Technique for MOS C-V and Surface State Measurements," Solid-State Electronics, Vol. 13, pp. 873-885, 1970.

93. Kuhn, M. and D. J. Silversmith "Ionic Contamination and Transport of Mobile Ions in MOS Structures," J. Electrochem. Soc., Vol. 118, No. 6, June 1971.

94. Lamb, D. R., G. R. Moghal, and R. J. Hawkins. "The Effect of Gold Doping on the Threshold Voltage, Hall Mobility, Gain, and Current Noise of MOS Transistors," Int. J. Electronics, Vol. 30, No. 2,, pp. 141-147, 1971.

95. Lane. C. H. "Stress at the Si-SiO_2 Interface and Its Relationship to Interface States," IEEE Trans. on Elect. Devices, ED-15, No. 12, December 1968.

96. Lane, C. H. "Reliability Problems with SiO_2 Passivation and Glassification," RADC-TR-72-55, March 1972.

97. Lane, C. H. "Aluminum Metallization and Contacts for Integrated Circuits," Metallurgical Trans., Vol. 1, March 1970.

98. Lee, H. S. "Metal-Oxide-Semiconductor Instability Produced by Electron Beam Evaporation of Aluminum Gates," IEEE Trans. on Elect. Devices, ED-25, No. 7, July 1978.

99. Lee, F. "Improved Radiation Hardness of Type 108 Linear Circuits," RCA report PRRL-76-CR-39, October 1976.

100. Lehovec, K. and A. Slobodskoy. "Impendence of Semiconductor Insulator Metal Capacitors," Solid-State Electronics, Vol. 7, pp. 59-79, 1964.

101. Lenglinger, M. and E. H. Snow. "Fowler-Nordheim Tunneling into Thermally Grown SiO_2," J. Appl. Phys., Vol. 40, No. 1, January 1969.

102. Li, S. P. and J. Maserjian. "Electron Radiation Effects on Time-Dependent Dielectric Breakdown in SiO_2 Films," Solid-State Electronics, Vol. 18 pp. 287-288, 1975.

103. Licciardello, D. C. and D. J. Thouless. " Conductivity and Mobility Edges for Two-Dimensional Disordered Systems," J. Phys. C: Solid-State Phys., Vol. 8, 1975.

104. Ma, T. P. and R. C. Barker. "Effect of Gamma-ray Irradiation on the Surface States of MOS Tunnel Junctions," J. Appl. Phys., Vol. 45, No. 1, January 1974.

105. Maier, R. J. "Time Dependence of the Interface State Density," AFWL Internal Report, 1973.

106. Maier, R. J. "A Study of Silicon Oxide Growth Mechanisms for the Purpose of Identifying Hardness Assurance Total Dose Screens," Air Force Weapons Laboratory report AFWL-TR-76-228, February 1977.

107. Maserjian, J. "Tunneling in Thin MOS Structures," J. Vac. Sci. Technology, Vol. II, No. 6, November/December 1974.

108. Mayo, S., R. Y. Koyama and T. F. Leedy, "Control of Mobile-Ion Contamination in Oxidation Ambients for MOS Device Processing," National Bureau of Stats., Report NBSIR-77-1404, January 1978.

109. McCaughan, D. V., R. A. Kushner, and V. T. Murphy. "Ion Neutralization Processes at Insulator Surfaces and Consequent Impurity Migration Effects in SiO_2 Films," Phys. Rev. Letters, Vol. 30, No. 13, March 1973.

110. McDonald, B. A. "Avalanche Degradation of h_{FE}," IEEE Trans. on Electron Devices, Vol. ED-17, No. 10, October 1970.

111. McMillan. "MOS [illegible] Techniques for IC Process Control," Solid-State Technology, September 1972.

112. McNutt, M. J. and C. T. Sah. "Experimental MOS C-V Data in Strong Inversion," IEEE Trans. on Elect. Devices, ED-25, No. 7, July 1978.

113. Mitchell, J. P. and D. G. Denure. "A Study of SiO_2 Layers on Si Using Cathodoluminescence Sprectra," Solid-State Electronics, Vol. 16, pp. 825-839, 1973.

114. Mitchell, J. P. "Radiation-Induced Space-Charge Buildup in MOS Structures," IEEE Trans. on Elect. Devices, Vol. ED-14, No. 11, November 1967.

115. Montillo, F. and P. Balk. "High Temperature Annealing of Oxidized Silicon Surfaces," J. Electrochem. Soc., Vol. 118, No. 9, September 1971.

116. Mott, N. F. "Silicon Dioxide and the Chalcogenide Semiconductors; Similarities and Differences," Advances in Physics, Vol. 26, No. 4, pp. 363-391, 1977.

117. Mott, N. F., M. Pepper, S. Pollitt, R. H. Wallis, and C. J. Adkins. "The Anderson Transition," Proc. of R. Soc. London A 345, pp. 169-205, 1975.

118. Myers, D. K. and R. W. Marshall, "Manufacturing Technology on Radiation-Hardened MSI/LSI Integrated Circuits," Air Force Materials Laboratory Report AFML-TR-76-73, May 1976.

119. Nassibian, A. G. and L. Faraone. "Nonequilibrium Response of MOS Devices to Linearly Varying Voltages," Appl. Phys. Letters, Vol. 32, No. 7, 1 April 1978.

120. Nauta, P. K. and M. W. Hillen. "Investigation of Mobile Ions in MOS Structures Using the TSIC Method," J. Appl. Phys., Vol. 49, No. 15, May 1978.

121. Nicollian, E. H. and H. Melchior. "A Quantitative Theory of 1/f Type Noise Due to Interface States in Thermally Oxidized Silicon," Bell Systems Technology Journal, November 1967.

122. Nicollian, E. H., C. N. Berglund, P. F. Schmidt, and J. M. Andrews. "Electrochemical Charging of Thermal SiO_2 Films by Injected Electron Currents," J. Appl. Phys., Vol. 42, No. 13, December 1971.

123. Nicollian, E. H. and A. Goetzberger. "The Si-SiO_2 Interface-Electrical Technique," Bell Systems Technology Journal, Vol. 46, No. 6, July/August 1967.

124. Oakley, R. E. and M. Pepper. "The Influence of Dielectric Charge on the Hole Field-Effect Mobility in Silicon Inversion Layers," Physics Letters, Vol. 41A, No. 1, August 1972.

125. Patel, J. R. and N. Kato. "X-ray Diffraction Topographs of Silicon Crystals with Superposed Oxide Film II Pendellosung Fringes: Comparison of Experiment with Theory," J. Appl. Phys., Vol. 44, No. 3, March 1973.

126. Pease, R. L. and J. P. Raymond. "Technology Assessment and Radiation Effects Characterization of Integrated Injection Logic." Defense Nuclear Agency Report DNA 4505F, April 1977.

127. Pease, R. L. "The Combined Effect of Ionizing Radiation and Bias Temperature Stressing on CMOS Inverters," Sandia Laboratories Report SLA-73-1122, December 1973.

128. Pease, R. L., F. N. Coppage, and E. D. Graham. "Dependence of Ionizing Radiation Induced h_{FE} Degradation on Emitter Periphery," IEEE Trans. on Nuclear Science NS-21, No. 2, April 1974.

129. Pease, R. L. and M. A. Ondrik. "Wafer and Diffusion Lot Dependence of Total Dose Degradation of Bipolar Transistors," Naval Weapons Support Center Report TR/7024/C75/314, 1975.

Pepper, M. "An Introduction to Silicon Inversion Layers," Contemporary Phys., Vol. 18, No. 5, 1977.

Pepper, M. "Electron Injection into SiO_2 from an Avalanching p-n [illegible]," J. Phys. D: Appl. Phys., Vol. 6, 1973.

132. Pepper, M. "Electron Injection into SiO_2 in the N-Channel Stacked Gate MOS Tetrode," IEEE Trans. on Elect. Devices, ED-21, No. 2, February 1974.

133. Pepper, M. and W. Eccleston. "Cation Transport in SiO_2," Phys. Stat. Sol., Vol. 12, p. 199, 1972.

134. Pepper, M. "Low Energy Electron Irradiation of the Si-SiO_2 Interface," Thin Solid Films, Vol. 14, pp. 57-510, 1972.

135. Pepper, M. "The Radiation Hardness of the Si-SiO_2 Interface and Carrier Localization in the Inversion Layer," J. Phys. C: Solid-State Phys., Vol. 10, 1977.

136. Pepper, M. "The Anderson Transistion in Silicon Inversion Layers: The Origin of the Random Field and the Effect of Substrate Bias," Proc. R. Soc. London, A.353, pp. 225-246, 1977.

137. Pepper, M., S. Pollitt, C. J. Adkins, and R. A. Stradling. "Anderson Localization in Silicon Inversion Layers," Critical Reviews in Solid-State Sciences, October 1975.

138. Pepper, M. "Magnetic Localization in Silicon Inversion Layers," Philosophical Magazine B, Vol. 37, No. 1, 1978.

139. Pepper, M. "Metals into Insulators," New Scientist, 15 December 1977.

140. Pepper, M., S. Pollitt, and C. J. Adkins. "The Spatial Extent of Localized State Wavefunctions in Silicon Inversions Layers," J. Phys. C: Solid-State Phys., Vol. 7, 1974.

141. Pierret, R. F. "The Gate-Controlled Diode so Measurement and Steady-State Lateral Current Flow in Deeply Depleted MOS Structures," Solid-State Electronics, Vol. 17, pp. 1257-1269, 1974.

142. Pierret, R. F. "Rapid Interpretation of the MOS-C C-t Transient," IEEE Trans. on Elect. Devices, ED-25, No. 9, September 1978.

143. Prince, J. L., J. J. Wortman, and J. R. Hanser. "On the Deeply Depleted MOS Capacitor," Proc. of IEEE, May 1970.

144. Reddi, V. G. K. "Influence of Surface Conditions on Silicon Planar Transistor Current Gain," Solid-State Electronics, V l. 10, 1967.

145. Repace, J. L. "The Effects of Ionizing Radiation on Mobile Ion Current Peaks in MOS Capacitors," IEEE Trans. on Elect. Devices, ED-25, No. 4, April 1978.

146. Revesz, A. G. "Noncrystalline Silicon Dioxide Films on Silicon: A Review," J. Noncrystalline Solids, Vol. II, 1973.

147. Rozgonyi, G. A. and R. A. Kushner. "The Elimination of Stacking Faults by Preoxidation Gettering of Silicon Wafers," Part II J. Electrochem. Soc., Vol. 123, No. 4, April 1976.

148. Rozgonyi, G. A. and C. W. Pearce. "Gettering of Surface and Bulk Impurities in Czochralski Silicon Wafers," Appl. Phys. Letters, Vol. 32, No. 11, June 1978.

149. Rozgonyi, G. A., P. M. Petroff, and M. H. Read. "Elimination of Oxidation Induced Stacking Faults by Preoxidation Gettering of Silicon Wafers," Part I J. Electrochem. Soc., Vol. 122, No. 12, December 1975.

150. Sah, C. T. and F. H. Hielscher. "Evidence of the Surface Origin of the 1/f Noise," Physical Review Letters, Vol. 17, No. 18, 31 October 1966.

151. Sakaki, H., K. Hoh, and T. Sugano. "Determination of Interface-State Density and Mobility Ratio in Silicon Surface Inversion Layers," IEEE Trans. on Elect. Devices, Vol. ED-17, No. 10, October 1970.

152. Saminadayar, K. and J. C. Pfister. "Surface-State Generation on MOS Capacitors Irradiated with UV Light and Electrons," Phys. Stat. Sol., Vol. 36, p. 679, 1976.

153. Saraswat, K. C. and J. D. Meindl. "Breakdown Walkout in Planar p-n Junctions," Solid-State Electronics, Vol. 21, pp. 813-819, 1978.

154. Schlesier, K. M. "Radiation Effects in Polysilicon-Gate CMOS," Rome Air Development Center Report RADC-TR-76-282, September 1976.

155. Schmidt, P. F. and W. Michel. "Anodic Formation of Oxide Films on Silicon," J. Electrochem. Soc., Vol. 104, No. 4, April 1957.

156. Schrieffer, J. R. "Effective Carrier Mobility in Surface-Space Charge Layers," Physical Review, Vol. 97, No. 3, February 1955.

157. Scoggan, G. A. and T. P. Ma. "Effects of Electron-beam Radiation on MOS Structures as Influenced by the Silicon Gopant," J. Appl. Phys., Vol. 48, No. 1, January 1977.

158. Share, S. and R. A. Martin. "Effects of Ionizing Radiation on Short Channel Thin Oxide (200-A) MOSFETS," IEEE Trans. on Electron Devices, August 1975.

159. Share, S., A. S. Epstein, V. Kumar, W. E. Dahlke, and W. Haller. "Effects of Ionizing Radiation on Thin-Oxide (20-1500 A) MOS Capacitors," J. Appl. Phys., Vol. 45, No. 11, November 1974.

160. Sher, A. and M. Lax. "Stochastic Transport in a Disordered Solid," Physical Review B, Vol. 7, No. 10, May 1973.

161. Schulz, M. and N. M. Johnson. "Transient Capacitance Measurements of Hole Emission from Interface States in MOS Structures," Appl. Phys. Letters, Vol. 31, No. 9, 1 November 1977.

162. Simmons, R. "Feasibility Study on Radiation Hardened Devices and Circuits," Plessey Co. Report DRIC-BR-38454, October 1973.

163. Simms, M. "Transient Surface Damage and Latchup in CMOS Devices," Research Triangle Inst. Report RTI-43U-991, June 1975.

164. Singh, B. R. and R. S. Srivastava. "Effects of Radiations on MOS Devices," Int. J. Electronics, Vol. 34, No. 6, pp. 785-793, 1973.

165. Sivo, L. L. and R. B. Greegor. "Service for Device Surface Analysis," Boeing Areospace Corp. Report D180-19044-1, September 1975.

166. Sivo, L. L. "Transistor Nonlinear Damage," Boeing Areospace Corp. Report D180-14225-1, May 1972.

167. Smith, J. S., D. D. Talada, and R. A. Blore. "MX-ACT I CMOS/SOS Reliability and Radiation Tolerance Study," Rome Air Development Center Report RADC-TR-77-301, September 1977.

168. Snow, E. H., A. S. Grove, and D. J. Fitzgerald. "Effects of Ionizing Radiation in Oxidized Silicon Surfaces and Planar Devices," Proc. of IEEE, Vol. 55, No. 7, July 1967.

169. Snow, E. H., A. S. Grove, B. E. Deal, and C. T. Sah. "Ion Transport Phenomena in Insulating Films," J. Appl. Phys., Vol. 36, No. 5, May 1965.

170. Solomon, P. "High Field Electron Trapping SiO_2," J. Appl. Phys., Vol. 48, No. 9, September 1977.

171. Stanley, A. G., K. E. Martin, W. E. Price, and M. K. Gauthier. "Total Dose Irradiation Effects Guidelines," 1st Draft prepared for Defense Nuclear Agency, September 1978.

172. Stanley, A. G., K. E. Martin, and W. E. Price. "Hardness Assurance for Total Dose Radiation," Jet Propulsion Lab Report 730-2, December 1977.

173. Stanley, A. G. and W. E. Price. "Irradiate-Anneal Screening of Total Dose Effects in Semiconductor Devices," Jet Propulsion Lab Report 33-788, July 1976.

174. Stanley, A. G., K. E. Martin, and W. E. Price. "Voyager Electronic Parts Radiation Program," Jet Propulsion Lab Report 77-41, September 1977.

175. Tangena, A. G., J. Middelhock, and N. F. de Rooy. "Influence of Positive Ions on the Current-Voltage Characteristics of MOS Structures," J. Appl. Physics, Vol. 49, No. 5, May 1978.

176. Terman, L. M. "An Investigation of Surface States at a Silicon/Silicon Oxide Interface Employing Metal-Oxide-Silicon Diodes," Solid-State Electronics, Vol. 5, pp. 285-299, 1962.

177. Verwey, J. F. "On the Mechanism of h_{FE} Degradation by Emitter-Base Reverse Current Stress," Microelectronics and Reliability, Vol. 9, pp. 425-432, 1970.

178. Verwey, J. F. "On the Emitter Degradation by Avalanche Breakdown in Planar Transistors," Solid-State Electronics, Vol. 14, pp. 775-782, 1971.

179. Verwey, J. F. "Avalanche-Injected Hole Current in SiO_2," Appl. Phys. Letters, Vol. 21, No. 9, November 1972.

180. Verwey, J. F. "Hole Currents in Thermally Grown SiO_2," J. Appl. Phys., Vol. 43, No. 5, May 1972.

181. Vinetskii, V. C., G. E. Chaika, and E. S. Shevchenko. "Charge and Potential Distribution in Dielectric Layers of MOS Structures Under Ionization," Phys. Stat. Sol., Vol. 26, p. 743, 1974.

182. Voland, G. and H. Pagnia. "Influence of X-irradiation on the Silicon-Silicon Dioxide Interface of MOS Structures," Appl. Phys. Letters, Vol. 3, pp. 77-80, 1974.

183. Wang, K. L. and A. O. Evweraye. "Determination of Interface and Bulk-Trap States of IGFET's Using Deep Level Transient Spectroscopy," J. Appl. Phys., Vol. 47, No. 10, October 1976.

184. Weinberg, Z. A., W. C. Johnson, and M. A. Lampert. "High Field Transport in SiO_2 on Silicon Induced by Corona Charging of the Unmetallized Surface," J. Appl. Phys., Vol. 47, No. 1, January 1976.

185. Weinberg, Z. A. and G. W. Rubloff. "Exiton Transport in SiO_2 as a Possible Cause of Surface-State Generation in MOS Structures," Appl. Phys. Letters, Vol. 32, No. 3, February 1978.

186. Wells, O. C. "An Irradiation Effect in Thermally Grown SiO_2," Appl. Phys. Letters, Vol. 14, No. 1, January 1969.

187. Whitefield, J. and H. D. Southward. "Investigation of Interface States Using MOS Transistors and Pulse Gate Techniques," University of New Mexico Report EE-244(77)AFWL-352-1, February 1977.

188. Williams, R. "Photoemission of Electrons from Silicon into Silicon Dioxide," Physical Review, Vol. 140, No. 2A, October 1965.

189. Williams. R. and M. H. Woods. "High Electric Fields in Silicon Dioxide Produced by Corona Charging," J. Appl. Phys., Vol. 44, No. 3, March 1973.

190. Williams, R. and M. H. Woods. "Laser-Scanning Photoemission Measurements of the Silicon-Silicon Dioxide Interface," J. Appl. Phys., Vol. 43, No. 10, October 1972.

191. Williams, R. and A. Willis. "Electron Multiplication and Surface Charge on Zime Oxide Single Crystals," J. Appl. Phys., Vol. 39, Nov. 8, July 1968.

192. Williams, R. and M. H. Woods. "Mobile Flouride Ions in SiO_2," J. Appl. Phys., Vol. 46, No. 2, February 1975.

193. Winokur, P. S. and M. M. Sokoloski. "Comparison of Interface-State Buildup in MOS Capacitors Subjected to Penetrating and Nonpenetrating Radiation," Appl. Phys. Letters, Vol. 28, No. 10, 15 May 1978.

194. Woods, M. H. and R. Williams. "Hole Traps in Silicon Dioxide," J. Appl. Phys., Vol. 47, No. 3, March 1976.

195. Yamashita, K., M Iwamoto, and T. Hino. "A Method for Studying Interface States in MIS Structures by Thermally Stimulated Surface Potential," J. Appl. Phys., Vol. 49, No. 5, May 1978.

196. Young, D. R. "Electrons Current Injected into SiO_2 From p-type Si Depletion Regions," J. Appl. Phys., Vol. 47, No. 5, May 1976.

197. Zaininger, K. H. and F. P. Haiman. "The C-V Technique as an Analytical Tool," Solid-State Technology, May 1970.

198. Zaininger, K. H. and G. Warfield. "Limitations of the MOS Capacitance Method for the Determination of Semiconductor Surface Properties," IEEE Trans. on Electron Devices, April 1965.

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Naval Surface Weapons Center
ATTN: Code F30
ATTN: Code F31

Naval Weapons Center
ATTN: Code 233

Naval Weapons Evaluation Facility
ATTN: Code AT-6

Naval Weapons Support Center
ATTN: Code 7024, J. Ramsey
ATTN: Code 7024, T. Ellis
ATTN: Code 70242, J. Munarin

Office of Naval Research
ATTN: Code 427, L. Cooper
ATTN: Code 220, D. Lewis

Office of the Chief of Naval Operations
ATTN: OP 985F

Strategic Systems Project Office
Department of the Navy
ATTN: NSP-2015
ATTN: NSP-2701, J. Pitsenberger
ATTN: NSP-230, D. Gold
ATTN: NSP-27331, P. Spector

DEPARTMENT OF THE AIR FORCE

Air Force Aero-Propulsion Laboratory
ATTN: POD, P. Stover

Air Force Avionics Laboratory
ATTN: TEA, R. Conklin
ATTN: DHE

Air Force Geophysics Laboratory
ATTN: SULL
ATTN: SULL Q-29

Air Force Institute of Technology
ATTN: ENP, J. Bridgeman

Air Force Materials Laboratory
ATTN: LTE
ATTN: LPO, R. Hickmott

Air Force Systems Command
ATTN: DLCAM, T. Seale
ATTN: DLCA
ATTN: DLW
ATTN: XRLA, R. Stead

Air Force Technical Applications Center
ATTN: TAE

Air Logistics Command
Department of the Air Force
ATTN: MMEDP
ATTN: MMEDD
ATTN: OO-ALC/MM, R. Blackburn

DEPARTMENT OF THE AIR FORCE (Continued)

Air Force Weapons Laboratory
Air Force Systems Command
ATTN: ELP, M. Knoll
ATTN: ELT, J. Ferry
ATTN: ELP, R. Maier
ATTN: ELP, G. Chapman
ATTN: ELP, J. Mullis
3 cy ATTN: SUL

Ballistic Missile Office
Air Force Systems Command
ATTN: MNNH, J. Tucker
ATTN: MNNG
ATTN: MNNL

Foreign Technology Division
Air Force Systems Command
ATTN: PDJV
ATTN: TQTD, B. Ballard

Headquarters Space Division
Air Force Systems Command
ATTN: [illegible] Kelly

Headquarters Space Division
Air Force Systems Command
ATTN: AQM
ATTN: AQT, W. Blakney

Headquarters Space Division
Air Force Systems Command
ATTN: DYS

Headquarters Space Division
Air Force Systems Command
ATTN: SZJ, R. Davis

Rome Air Development Center
Air Force Systems Command
ATTN: RBRP, C. Lane
ATTN: RBRM, J. Brauer

Rome Air Development Center
Air Force Systems Command
ATTN: ESR, P. Vail
ATTN: ESR, W. Shedd
ATTN: ESE, A. Kahan
ATTN: ETS, R. Dolan
ATTN: ESER, K. Buchanan

Strategic Air Command
Department of the Air Force
ATTN: XPFS, M. Carra

DEPARTMENT OF ENERGY

Department of Energy
Albuquerque Operations Office
ATTN: Document Control for WSSB

DEPARTMENT OF ENERGY CONTRACTORS

Lawrence Livermore Laboratory
ATTN: Technical Information Dept.

Los Alamos Scientific Laboratory
ATTN: J. Freed

DEPARTMENT OF ENERGY CONTRACTORS (Continued)

Sandia Laboratories
ATTN: F. Coppage
ATTN: W. Dawes
ATTN: J. Hood
ATTN: R. Gregory
ATTN: J. Barnum

OTHER GOVERNMENT AGENCIES

Central Intelligence Agency
ATTN: OSI/MTD, A. Padgett
ATTN: OSI/RD

Department of Commerce
National Bureau of Standards
ATTN: Security Officer for J. Humphreys
ATTN: Security Officer for W. Bullis
ATTN: Security Officer for K. Galloway
ATTN: Security Officer for J. Mayo-Wells
ATTN: Security Officer for J. French
ATTN: Security Officer for S. Chappell
ATTN: Security Officer for R. Scace

NASA
Goddard Space Flight Center
ATTN: V. Danchenko
ATTN: J. Adolphsen

NASA
George C. Marshall Space Flight Center
ATTN: L. Haniter
ATTN: M. Nowakowski
ATTN: EG02
ATTN: B. Yearwood

NASA
ATTN: J. Murphy

NASA
Lewis Research Center
ATTN: M. Braddour

NASA
Ames Research Center
ATTN: G. DeYoung

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Advanced Microdevices, Inc.
ATTN: J. Schlageter

Advanced Research & Applications Corp.
ATTN: R. Armistead
ATTN: L. Palcuti

Aerojet Electro-Systems Co.
ATTN: T. Hanscome

Aerospace Corp.
ATTN: S. Bower
ATTN: W. Willis
ATTN: D. Fresh

Aerospace Industries Assoc. of America, Inc.
ATTN: C. Siegel

Battelle Memorial Institute
ATTN: R. Thatcher

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

BDM Corp.
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ATTN: D. Alexander
ATTN: D. Wunch

Bendix Corp.
ATTN: E. Meeder

Boeing Co.
ATTN: D. Egelkrout

Boeing Co.
ATTN: C. Rosenberg
ATTN: W. Rumpza
ATTN: I. Arimura
ATTN: A. Johnston
ATTN: C. Dixon

Burr-Brown Research Corp.
ATTN: H. Smith

California Institute of Technology
ATTN: A. Shumka
ATTN: A. Stanley
ATTN: W. Price

Charles Stark Draper Lab., Inc.
ATTN: P. Greiff
ATTN: A. Schutz
ATTN: R. Bedingfield
ATTN: C. Lai
ATTN: R. Ledger

Cincinnati Electronics Corp.
ATTN: L. Hammond
ATTN: C. Stump

Control Data Corp.
ATTN: J. Meehan

University of Denver
ATTN: Security Officer for F. Venditti

E-Systems, Inc.
ATTN: K. Reis

Electronic Industries Association
ATTN: J. Hessman

EMM Corp.
ATTN: F. Frch

Exp. & Math Physics Consultants
ATTN: T. Jordan

Fairchild Camera and Instrument Corp.
ATTN: Sec. Cor. for D. Myers
ATTN: R. Marshall

Ford Aerospace & Communications Corp.
ATTN: J. Davison
ATTN: Technical Information Services

Ford Aerospace & Communications Corp.
ATTN: J. Cadle

Franklin Institute
ATTN: R. Thompson

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Garrett Corp.
ATTN: R. Weir

General Dynamics Corp.
ATTN: W. Hansen
ATTN: N. Cohn

General Dynamics Corp.
ATTN: R. Fields
ATTN: O. Wood

General Electric Co.
ATTN: J. Andrews
ATTN: R. Casey
ATTN: J. Peden

General Electric Co.
ATTN: J. Palchefsky, Jr.
ATTN: W. Patterson
ATTN: Technical Library
ATTN: R. Casey
ATTN: R. Benedict

General Electric Co.
ATTN: J. Reidl

General Electric Co.
ATTN: R. Hellen

General Electric Co.
ATTN: J. Gibson
ATTN: D. Cole

General Electric Co.
ATTN: D. Pepin

General Electric Company—TEMPO
ATTN: DASIAC
ATTN: M. Espig

General Electric Company—TEMPO
ATTN: DASIAC

General Research Corp.
ATTN: R. Hill
ATTN: Technical Information Office

George C. Messenger
Consulting Engineer
ATTN: G. Messenger

Georgia Institute of Technology
ATTN: R. Curry

Georgia Institute of Technology
ATTN: Res. & Sec. Coord. for M. Denny

Goodyear Aerospace Corp.
ATTN: Security Control Station

Grumman Aerospace Corp.
ATTN: J. Rogers

GTE Sylvania, Inc.
ATTN: L. Blaisdell
ATTN: C. Thornhill
ATTN: L. Paupler

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

GTE Sylvania, Inc.
ATTN: H & V Group
ATTN: P. Fredrickson
ATTN: H. Ullman
ATTN: J. Waldron

Harris Corp.
ATTN: T. Sanders
ATTN: J. Cornell
ATTN: C. Anderson

Honeywell, Inc.
ATTN: R. Gumm

Honeywell, Inc.
ATTN: C. Cerulli

Honeywell, Inc.
ATTN: Technical Library

Honeywell, Inc.
ATTN: K. Gaspard

Hughes Aircraft Co.
ATTN: J. Singletary
ATTN: R. McGowan

Hughes Aircraft Co.
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ATTN: W. Scott
ATTN: E. Smith

IBM Corp.
ATTN: T. Martin
ATTN: H. Mathers
ATTN: F. Tietse

IIT Research Institute
ATTN: I. Mindel

Institute for Defense Analyses
ATTN: [illegible]

Intel Corp.
ATTN: M. Jordan

International Business Machines Corp.
ATTN: [illegible]

International Tel. & Telegraph Corp.
ATTN: [illegible]
ATTN: A. Richardson

Intersil, Inc.
ATTN: [illegible]

IRT Corp.
ATTN: [illegible]

JAYCOR
ATTN: [illegible]
ATTN: [illegible]
ATTN: [illegible]

Johns Hopkins University
ATTN: [illegible]

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Kaman Sciences Corp.
ATTN: J. Lubell
ATTN: P. Jessen
ATTN: M. Bell

Litton Systems, Inc.
ATTN: G. Maddox
ATTN: J. Retzler

Lockheed Missiles & Space Co., Inc.
ATTN: J. Smith
ATTN: J. Crowley

Lockheed Missiles & Space Co., Inc.
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ATTN: C. Thompson
ATTN: P. Bene
ATTN: E. Smith
ATTN: H. Phillips
ATTN: E. Hessee

M.I.T. Lincoln Lab.
ATTN: P. McKenzie

Magnavox Govt. & Indus. Electronics Co.
ATTN: W. Richeson

Martin Marietta Corp.
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ATTN: H. Cates
ATTN: W. Janocko
ATTN: R. Gaynor

Martin Marietta Corp.
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McDonnell Douglas Corp.
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ATTN: Library
ATTN: D. Dohm

McDonnell Douglas Corp.
ATTN: D. Fitzgerald
ATTN: J. Holmgrem

McDonnell Douglas Corp.
ATTN: Technical Library

Mission Research Corp.
ATTN: C. Longmire

Mission Research Corp.
ATTN: R. Pease

Mission Research Corporation—San Diego
ATTN: J. Azarewicz
ATTN: R. Berger
ATTN: J. Raymond
ATTN: V. Van Lint

Mitre Corp.
ATTN: M. Fitzgerald

Motorola, Inc.
ATTN: A. Christensen

Motorola, Inc.
ATTN: L. Clark

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

National Academy of Sciences
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National Semiconductor Corp.
ATTN: R. Wang
ATTN: A. London

University of New Mexico
ATTN: H. Southward

Northrop Corp.
ATTN: P. Eisenberg
ATTN: J. Srour
ATTN: T. Jackson

Northrop Corp.
ATTN: D. Strobel
ATTN: P. Gardner
ATTN: L. Apodaca

Physics International Co.
ATTN: Division 6000
ATTN: J. Huntington
ATTN: J. Shea

R & D Associates
ATTN: R. Poll
ATTN: C. MacDonald
ATTN: S. Rogers

Rand Corp.
ATTN: C. Crain

Ratheon Co.
ATTN: J. Ciccio

Ratheon Co.
ATTN: H. Flescher
ATTN: A. Van Doren

RCA Corp.
ATTN: V. Mancino
ATTN: G. Brucker

RCA Corp.
ATTN: D. O'Connor
ATTN: Office N103

RCA Corp.
ATTN: R. Killion

RCA Corp.
ATTN: E. Van Keuren
ATTN: J. Saultz

RCA Corp.
ATTN: W. Allen

Rensselaer Polytechnic Institute
ATTN: R. Gutmann

Research Triangle Institute
ATTN: Sec. Office for M. Simons, Jr.

Rockwell International Corp.
ATTN: T. Oki
ATTN: V. Strahan
ATTN: V. De Martino
ATTN: G. Messenger
ATTN: J. Bell

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Rockwell International Corp.
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Rockwell International Corp.
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ATTN: TIC BA08

Sanders Associates, Inc.
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Science Applications, Inc.
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ATTN: J. Naber
ATTN: V. Ophan
ATTN: D. Long

Science Applications, Inc.
ATTN: W. Chadsey

Science Applications, Inc.
ATTN: D. Stribling

Singer Co.
ATTN: J. Brinkman

Singer Co.
ATTN: R. Spiegel

Solar Energy Research Institute
ATTN: A. Stanley

Sperry Rand Corp.
ATTN: Engineering Laboratory

Sperry Rand Corp.
ATTN: C. Craig
ATTN: P. Maraffino
ATTN: F. Scaravaglione
ATTN: R. Viola

Sperry Rand Corp.
ATTN: D. Schow

Sperry Univac
ATTN: J. Inda

Spire Corp.
ATTN: R. Little

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

SRI International
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ATTN: A. Whitson
ATTN: P. Dolan

Systron-Donner Corp.
ATTN: J. Indelicato

Teledyne Ryan Aeronautical
ATTN: J. Rawlings

Texas Instruments, Inc.
ATTN: A. Peletier
ATTN: R. Stehlin

Texas Instruments, Inc.
ATTN: F. Poblenz

TRW Defense & Space Sys. Group
ATTN: R. Kingsland
ATTN: A. Pavelko
ATTN: A. Witteles
ATTN: P. Guilfcyle
ATTN: O. Adams
ATTN: H. Holloway

TRW Defense & Space Sys. Group
ATTN: F. Fay
ATTN: R. Kitter
ATTN: M. Gorman

TRW Systems and Energy
ATTN: G. Spehar
ATTN: B. Gililland
ATTN: D. Millward

Vought Corp.
ATTN: Library
ATTN: Technical Data Center
ATTN: R. Tomme

Westinghouse Electric Co.
ATTN: L. McPherson

Westinghouse Electric Corp.
ATTN: H. Kalapaca
ATTN: D. Crichi